

Model Name: 8AENXP-D Revision 1.01

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02	BLOCK DIAGRAM
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06	P4_LGA775_C
07	P4_LGA775_D
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09	GMCH-GARNTSDALE_DDR
10	GMCH-GRANTS DALE_PCI E, DMI
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12	GMCH-GRANTS DALE_GND
13	GMCH-GRANTS DALE_PWR
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22	ICH6 VCC, GND
23	FWH
24	GB/CK410M CLOCK.
25	PCI SLOT 1, 2,3
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27	H/W MONITOR

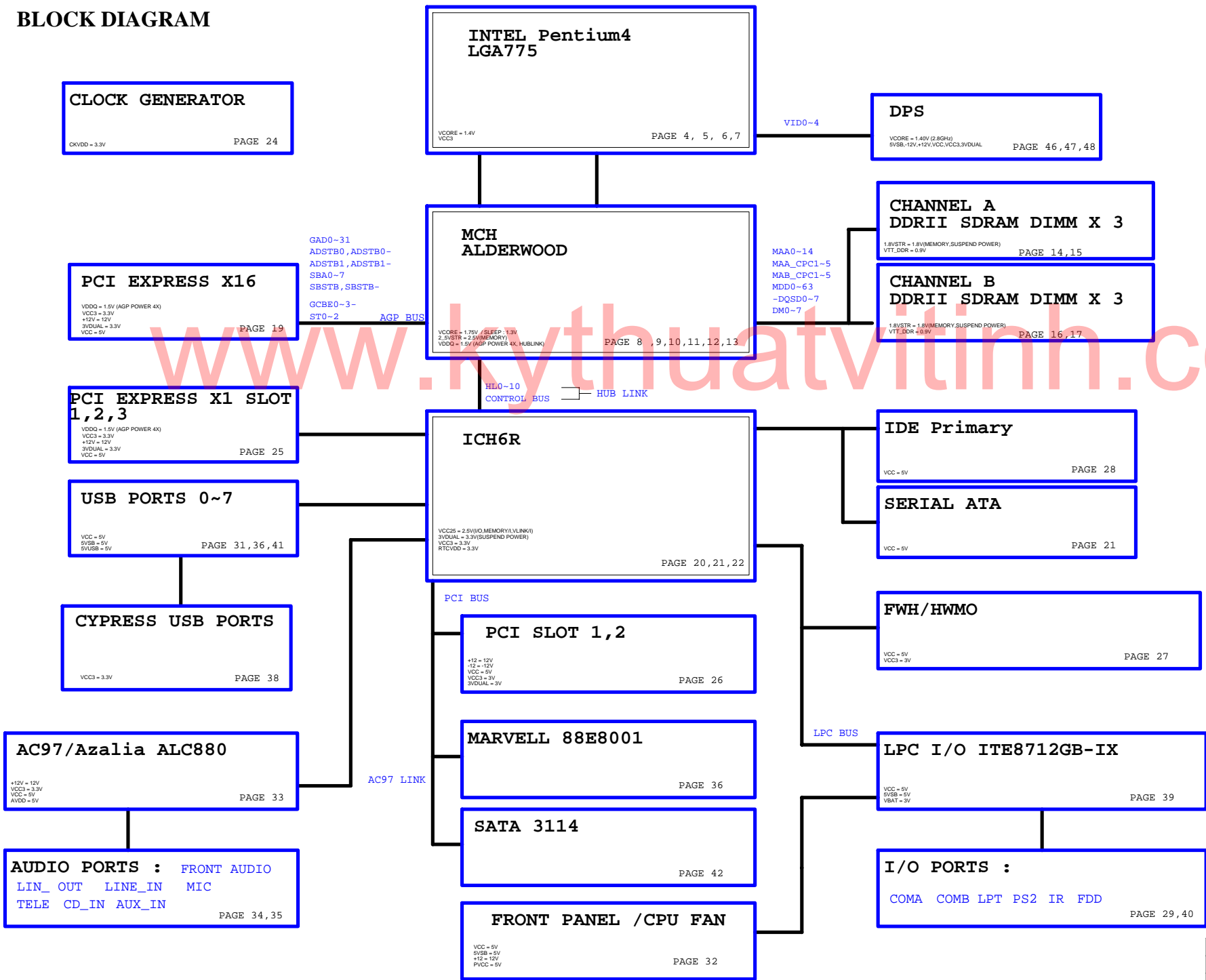
SHEET TITLE

28	IDE
29	KB_PS2,GAME PORT
30	FRONT PANEL
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39	ITE 8712GB
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43	TI 1394B-1
44	TI 1394B-2
45	ATX POWER CONN.
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47	DPS-2
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Cover Sheet			
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BLOCK DIAGRAM





**Version: 1.01**

## Component value change history

Data	Change Item	Reason
01'05'04	1.Remove High Side MoSFET	
	2.Change Q45 to SUD50N024-09P	
	3.Rmove MOSFET HSINK	
	4. Approve LAN Power	
01'08'04	1.Change MOSFET Gate from 0/6 to 1/6	
	2.Remove EC80,EC35,EC45,EC71,EC70,EC72,EC74,LEC9,EC61,EC79	
	3.Change U24 to 10HL6-184201-10 ICS CK410M	
	4.Change U17 to 10GL4-15b252-10	
	5.Change DU3 to 10TA1-0F8266-10	
02'18'04	1.Change GMCH to A2	
	2.Change ICH6 to A1	
	3.Change CLOCK GEN. to ICS 954271	
	4.Remove Onboard DPS	
	5. Add PROCESSOR HOT CIRCUIT	
04'22'04	1.Change GMCH to B0	
	2.Change ICH6 to B0	
	3.Change On-Lan to Broadcom 5751	
	4.Change PCB to 0.3	
05'11'04	1.Change GMCH to B1	
	2.Chabge ICH6 to B1	
	2.Change BCM5751 to A1	
	4.Change PCB to 1.0	
05'17'04	1.Change C256 0.1U to C256 100	
05'18'04	1.Remove U77,U78 Socket	
	2.Add L15,L10替料	
05'20'04 1.0C ECN	1.Remove DQ43	
	2.Remove DR219	
	3.Change CU1 to P/N:10HP5-366880-31	
	4.Add ITE8712F/IX3替料	
	5.Remove BU1,PCI_BT,R552	
05'31'04 1.0C ECN	1.Add DU5 LM324 TI 替料	

Circuit or PCB layout change  
for next version

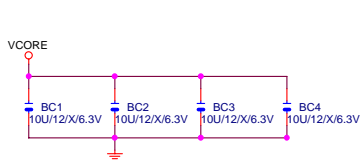
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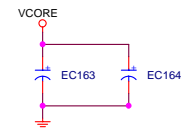
Title	BOM & PCB MODIFY HISTORY
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Size Custom	Document Number <b>8AENXP-D</b>	Rev <b>1.01</b>
Date: Wednesday, November 24, 2004	Sheet 3 of 48	

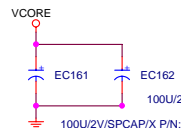




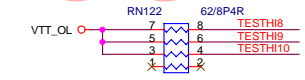
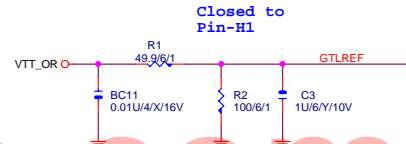
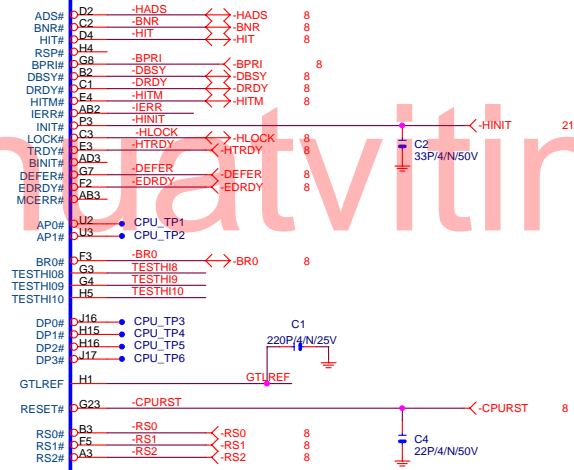
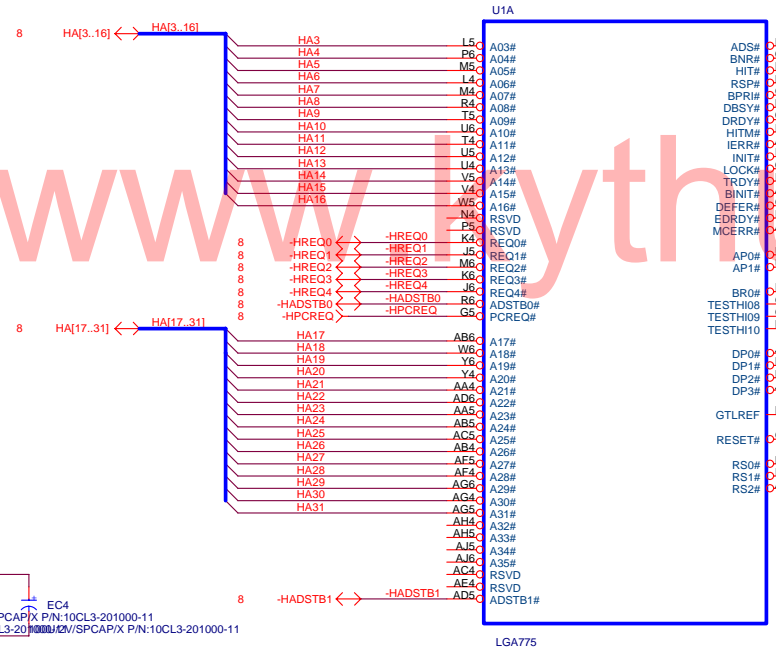
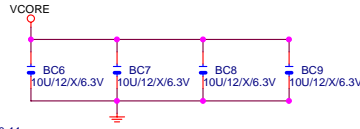
100U/2V/SPCAP/X P/N:10CL3-201000-11



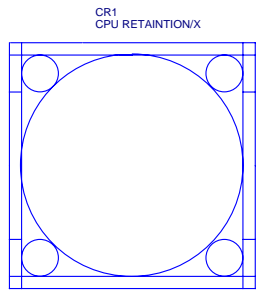
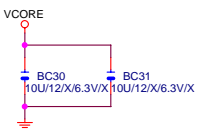
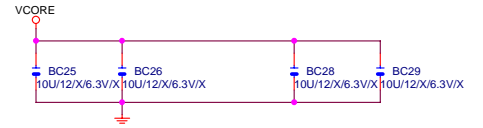
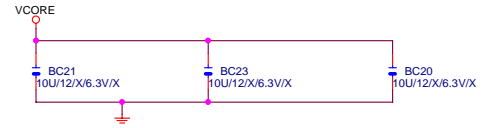
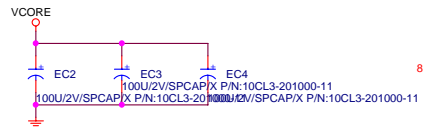
100U/2V/SPCAP/X P/N:10CL3-201000-11



100U/2V/SPCAP/X P/N:10CL3-201000-11



SP-CAP X 4PCS









**Note:**  
VCCA & VCOREPLL  
define doesn't same as  
old P4 design kit

As close as possible to  
CPU socket

Trace width doesn't  
less than 12 Mil

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P4\_LGA775-B

8AENXP-D

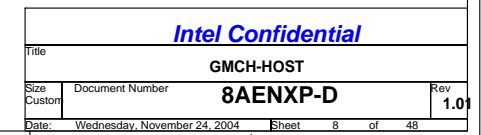
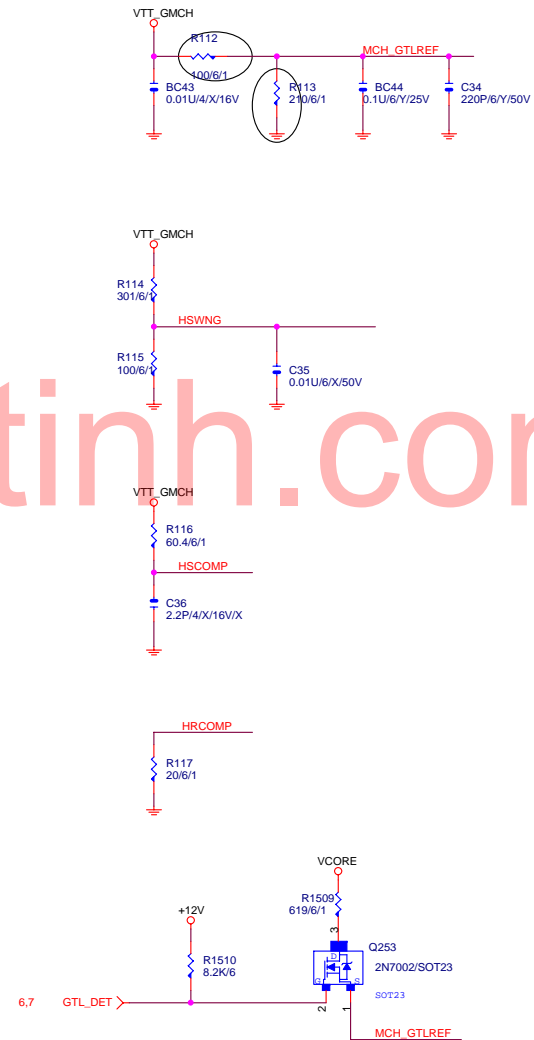
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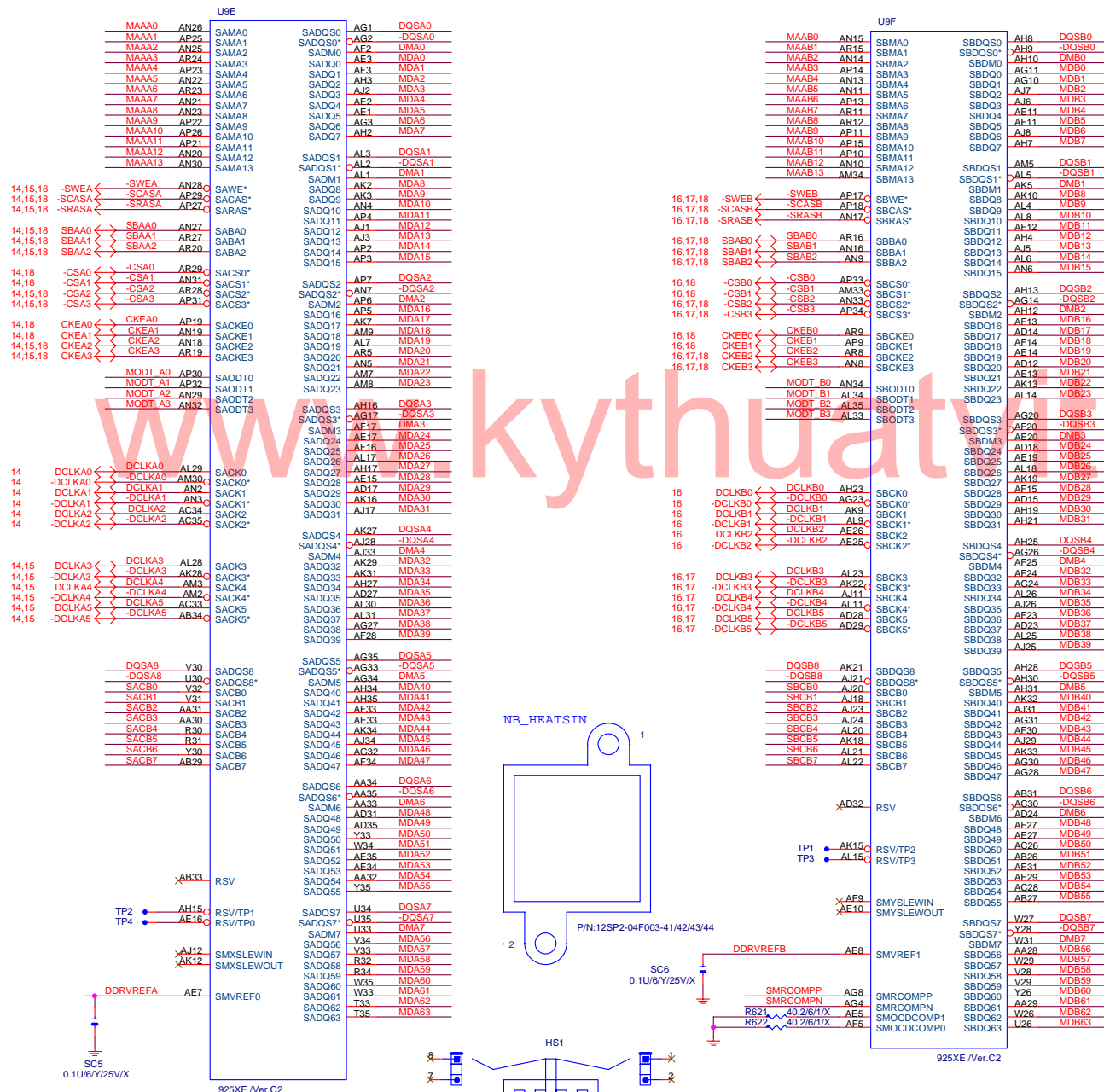






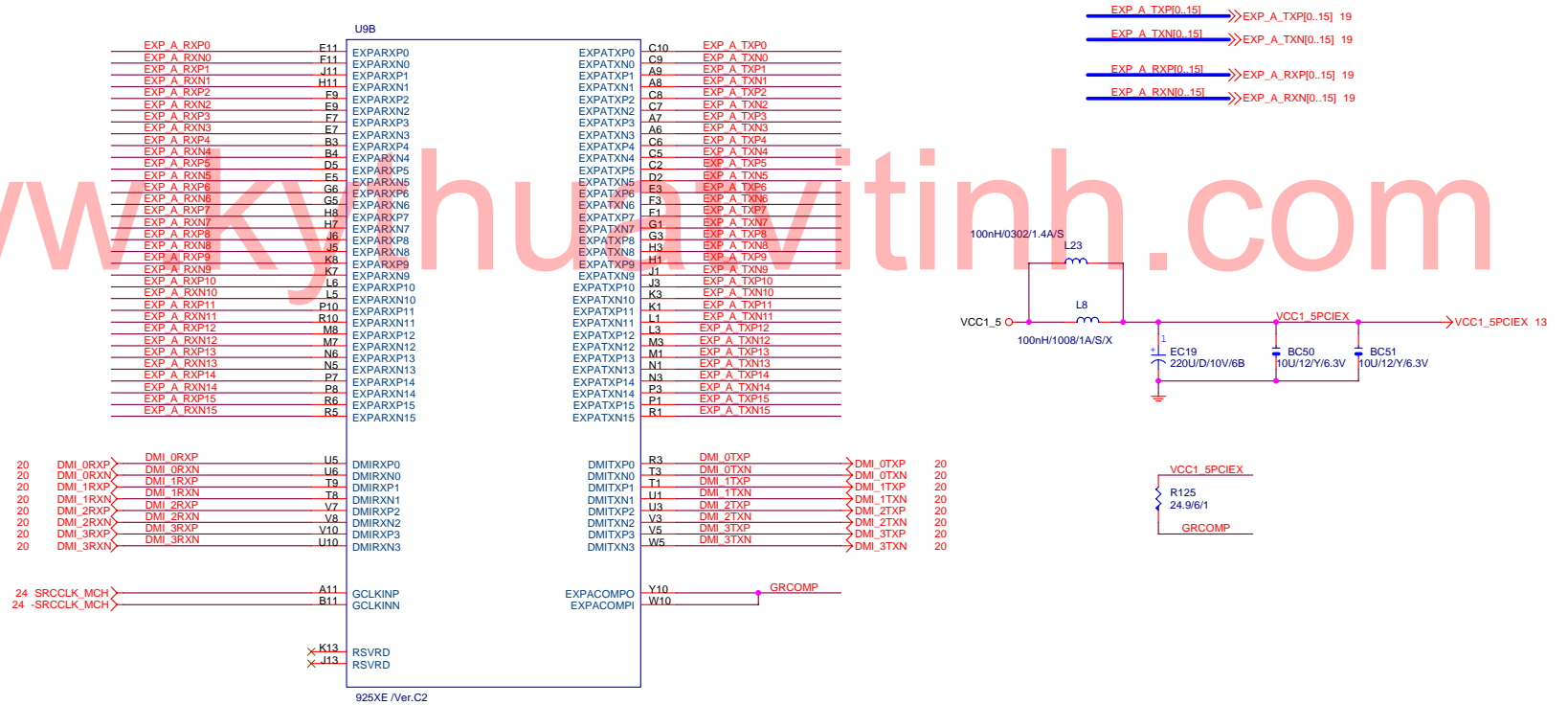
MODT\_A[0..3] ↔ MODT\_A[0..3] 14,15,18

MODT\_B[0..3] ↔ MODT\_B[0..3] 16,17,18

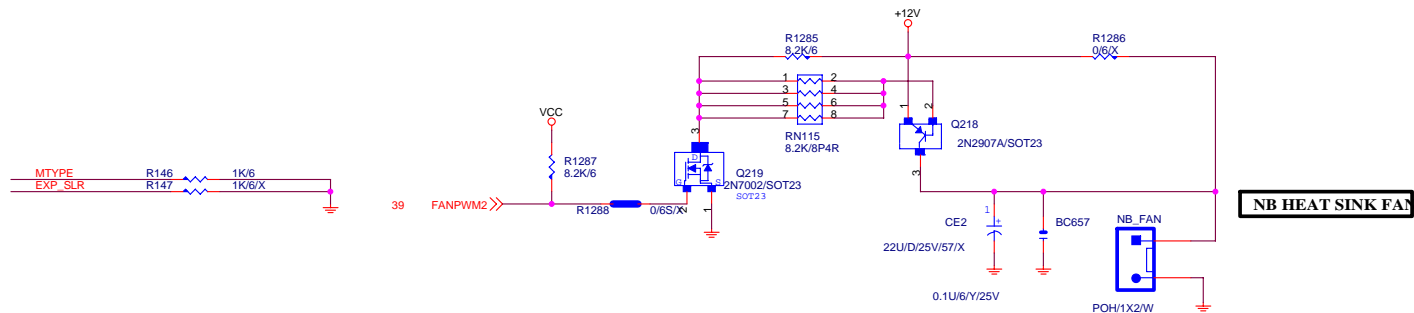




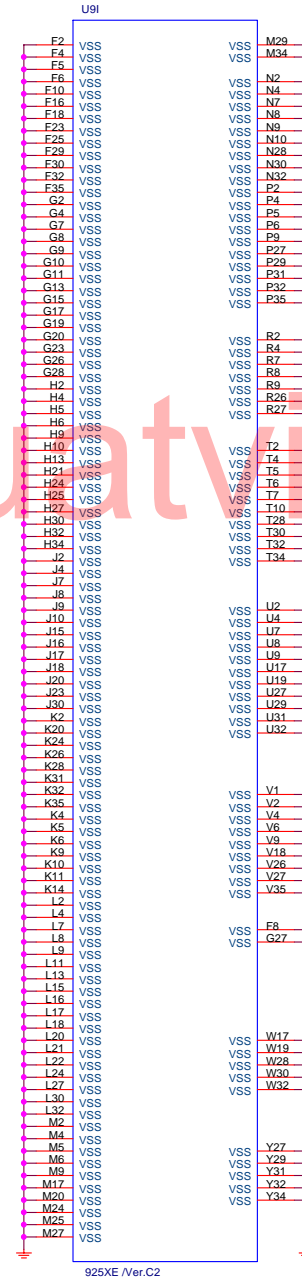
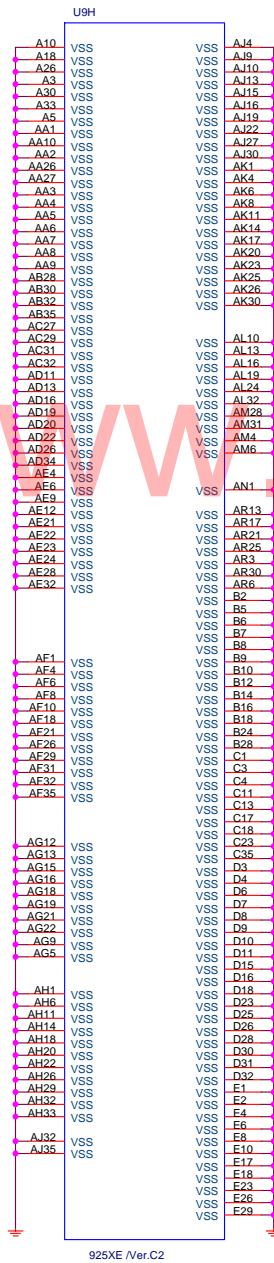
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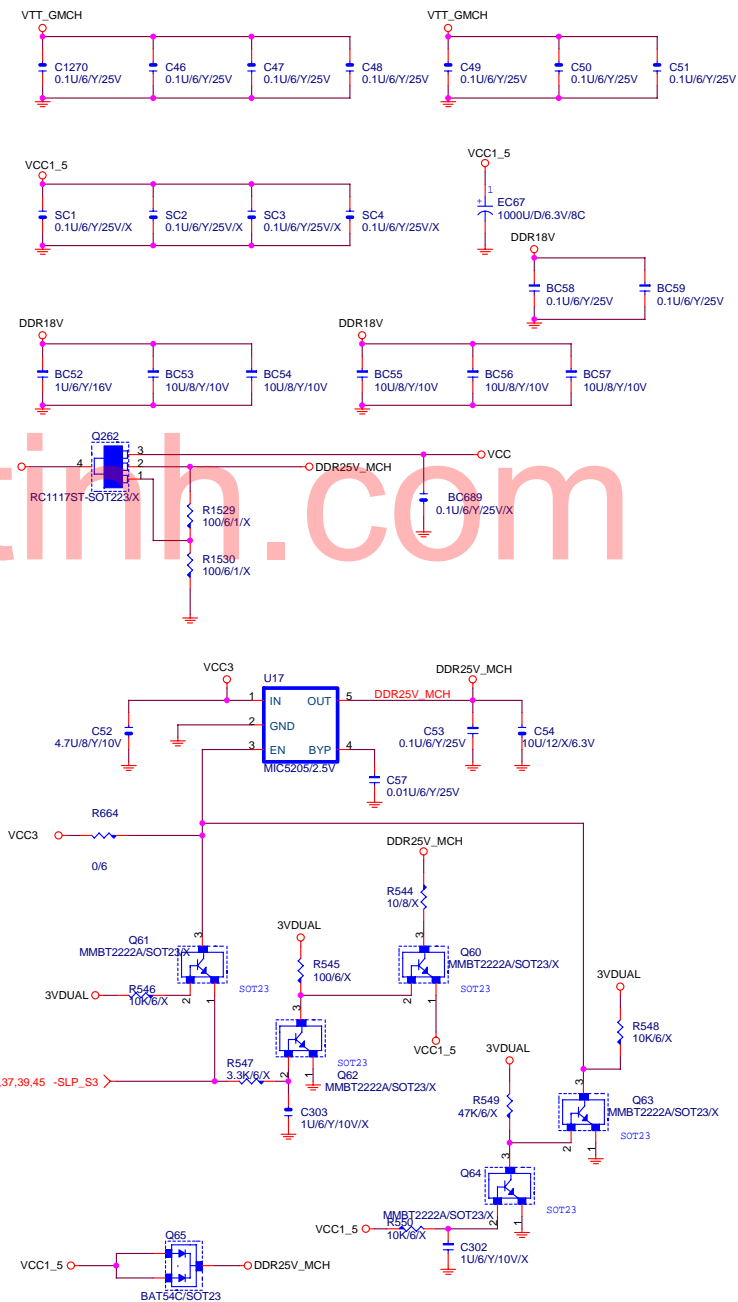
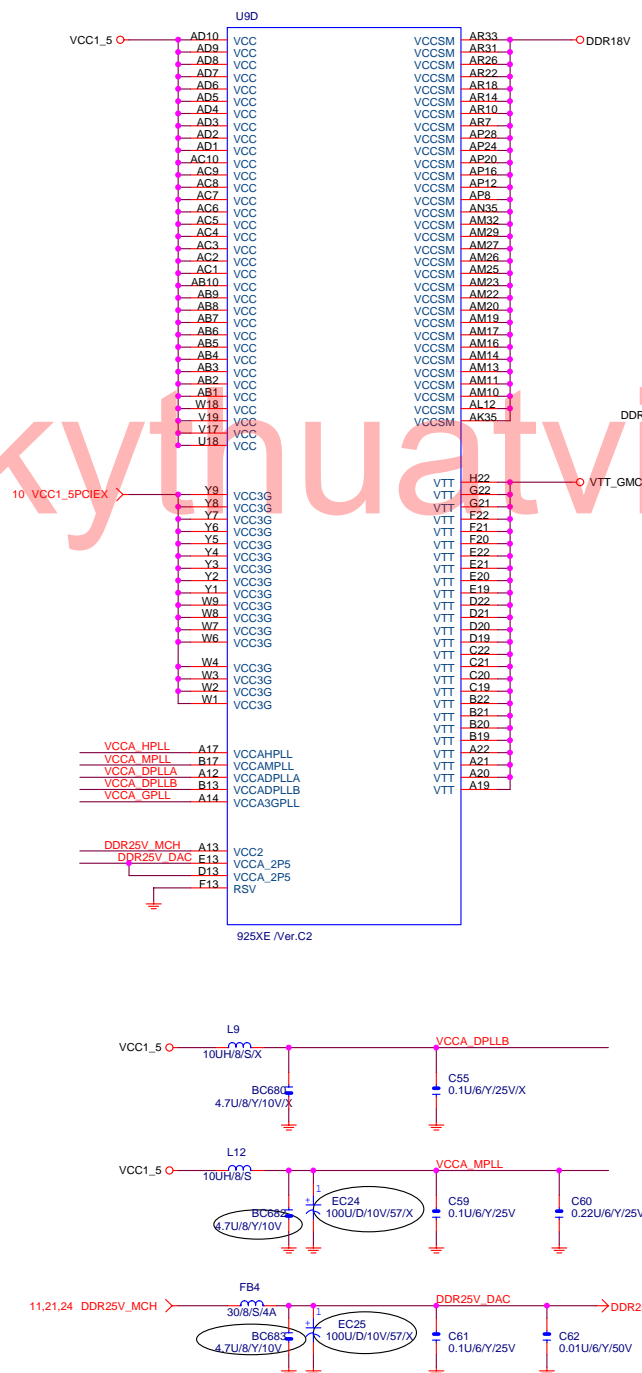




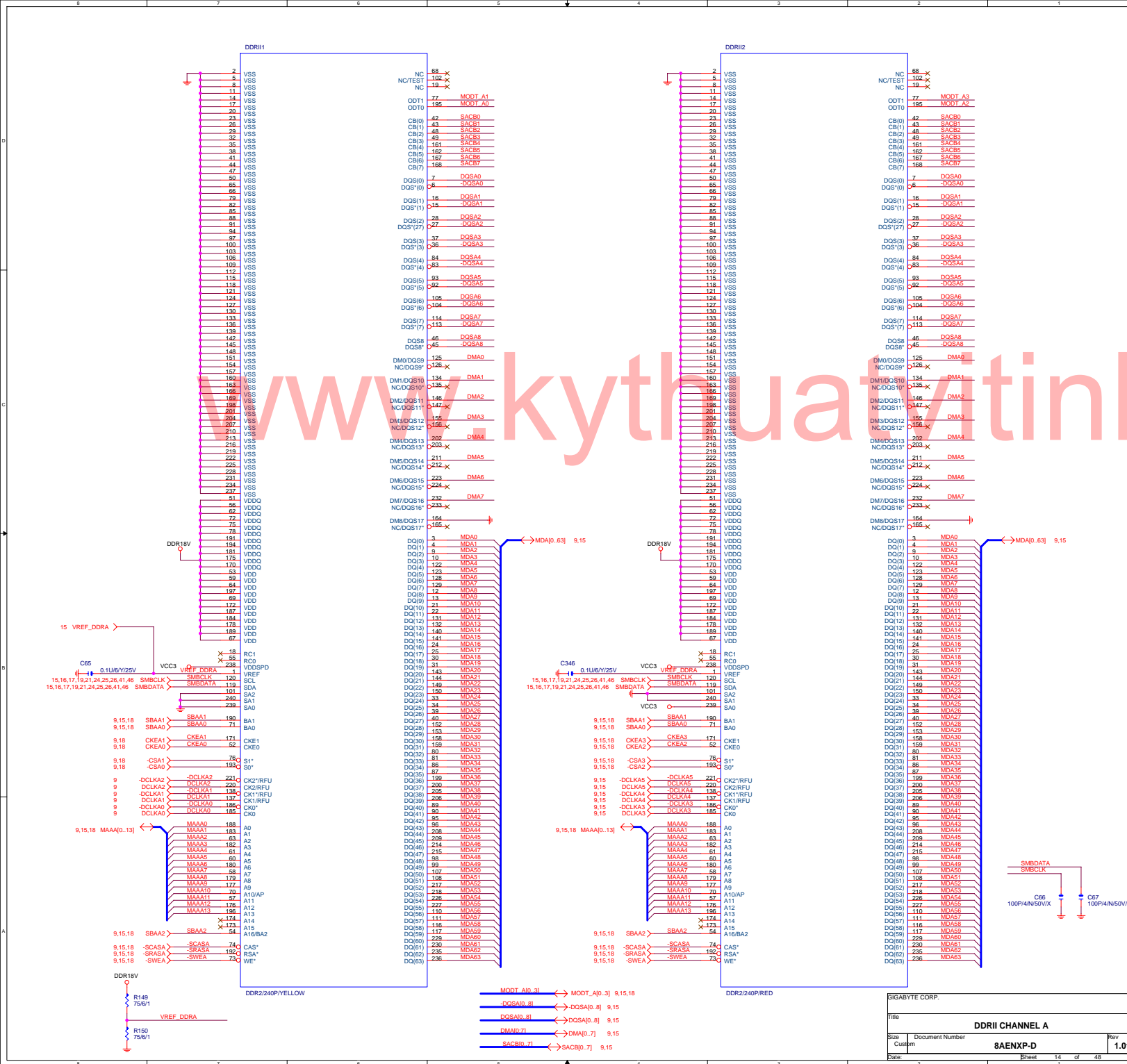














MODT\_A[0..3] ↔ MODT\_A[0..3] 9,14,18  
-DQSA[0..8] ↔ DQSA[0..8] 9,14  
DQSA[0..8] ↔ DQSA[0..8] 9,14  
DMA[0..7] ↔ DMA[0..7] 9,14  
SACB[0..7] ↔ SACB[0..7] 9,14

14 VREF\_DDRA

C1255

0.1uF/25V

VCC3

VREF\_DDRA

SMBCLK

SMBDATA

SMBDATA

VCC3

SBA1

SBA0

CKEA2

CKEA3

CSA2

CSA3

-DCLKA5

-DCLKA6

-DCLKA7

-DCLKA8

-DCLKA9

-DCLKA10

-DCLKA11

-DCLKA12

-DCLKA13

-DCLKA14

-DCLKA15

-DCLKA16

-DCLKA17

-DCLKA18

-DCLKA19

-DCLKA20

-DCLKA21

-DCLKA22

-DCLKA23

-DCLKA24

-DCLKA25

-DCLKA26

-DCLKA27

-DCLKA28

-DCLKA29

-DCLKA30

-DCLKA31

-DCLKA32

-DCLKA33

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-DCLKA208

-DCLKA209

-DCLKA210

-DCLKA211

-DCLKA212

-DCLKA213

-DCLKA214

-DCLKA215

-DCLKA216

-DCLKA217

-DCLKA218

-DCLKA219

-DCLKA220

-DCLKA221

-DCLKA222

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-DCLKA263

-DCLKA264

-DCLKA265

-DCLKA266

-DCLKA267

-DCLKA268

-DCLKA269

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-DCLKA271

-DCLKA272

-DCLKA273

-DCLKA274

-DCLKA275

-DCLKA276

-DCLKA277

-DCLKA278

-DCLKA279

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-DCLKA284

-DCLKA285

-DCLKA286

-DCLKA287

-DCLKA288

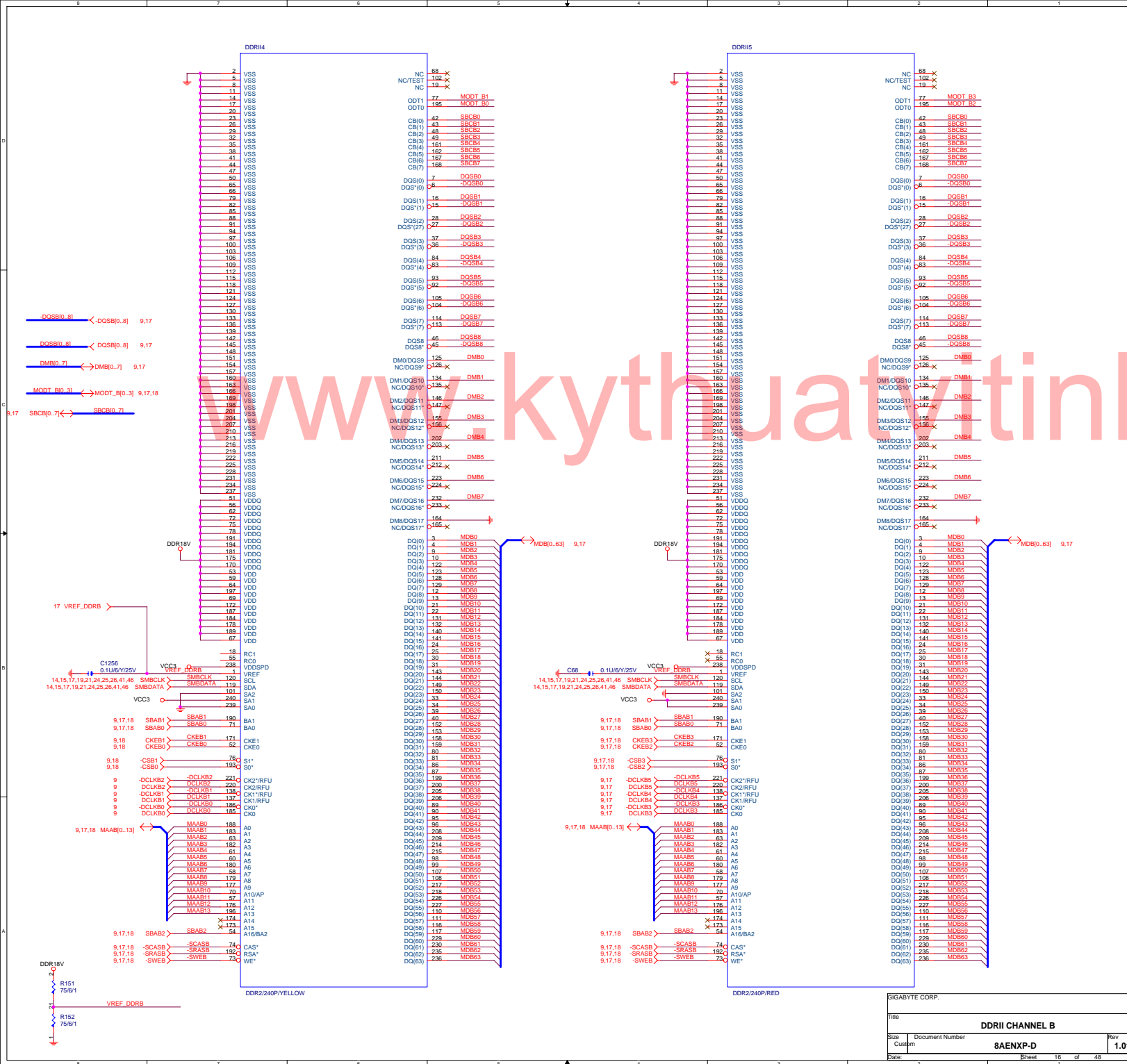
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-DCLKA290

-DCLKA291

-DCLKA292







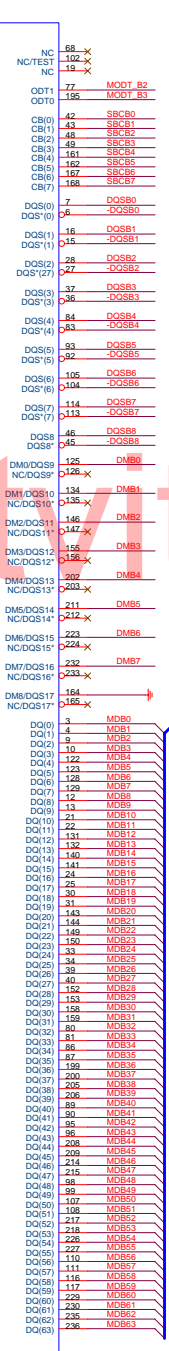
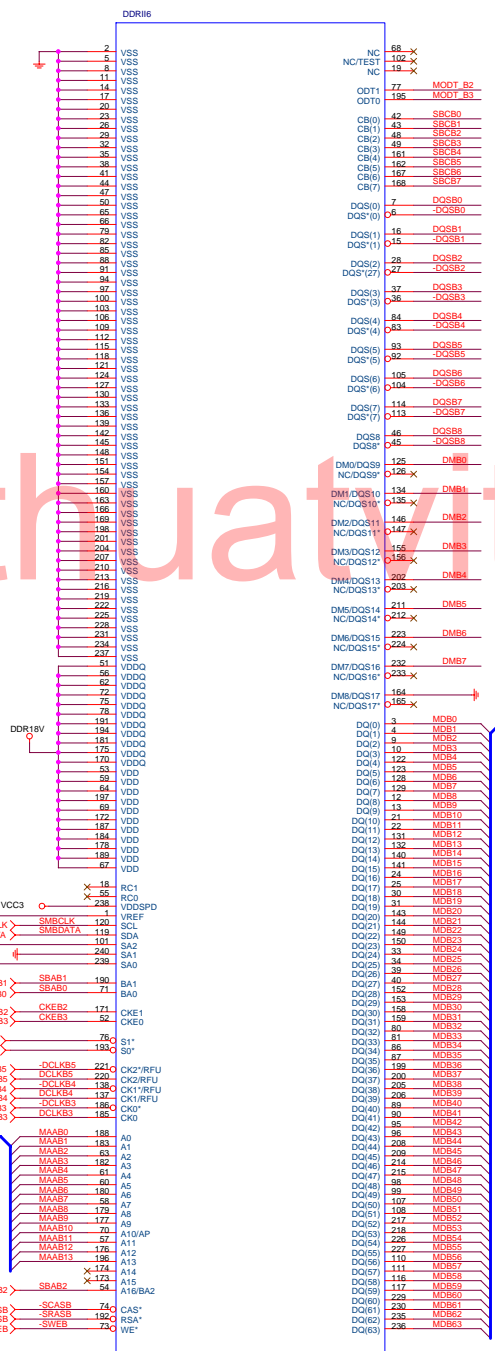
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DQSBI0\_#1 < DQSBI0\_#1 9.16  
DQSBI0\_#1 < DQSBI0\_#1 9.16  
DMBI0\_71 < DMBI0\_71 9.16  
MODT\_BIO\_31 < MODT\_BIO\_31 9.16,18  
9.16 SBCE0\_71 < SBCE0\_71

16 VREF\_DDRB

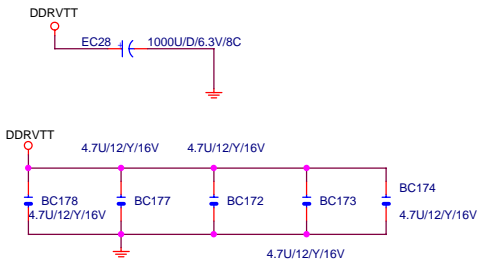
C1259 0.1uF/25V  
VCC3  
14,15,16,19,21,24,25,26,41,46 SMBCLK  
14,15,16,19,21,24,25,26,41,46 SMBDATA  
VCC3

9.16,18 SBAB1  
9.16,18 SBAB0  
9.16,18 CKEB2  
9.16,18 CKEB3  
9.16,18 CSB2  
9.16,18 CSB3  
9.16 DCLKB5  
9.16 DCLKB6  
9.16 DCLKB4  
9.16 DCLKB3  
9.16 DCLKB2  
9.16,18 MAAB0  
9.16,18 MAAB1  
9.16,18 MAAB2  
9.16,18 MAAB3  
9.16,18 MAAB4  
9.16,18 MAAB5  
9.16,18 MAAB6  
9.16,18 MAAB7  
9.16,18 MAAB8  
9.16,18 MAAB9  
9.16,18 MAAB10  
9.16,18 MAAB11  
9.16,18 MAAB12  
9.16,18 MAAB13  
9.16,18 SBAB2  
9.16,18 SCASB  
9.16,18 SRASB  
9.16,18 SWEB

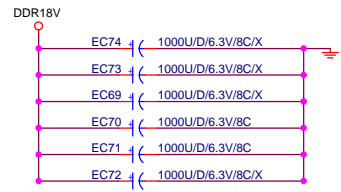




## DDRVTT Decouple



## DDR TERMINATION CHANNEL A

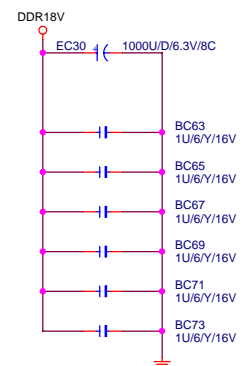


DDRVTT

MODT_A0	R542	39/4
MODT_A1	R543	39/4
MODT_A2	R610	39/4
MODT_A3	R613	39/4
MAAA8	R611	33/4
MAAA7	R614	33/4
MAAA4	R596	33/4
MAAA1	R595	33/4
MAAA13	R599	33/4
MAAA2	R618	33/4
MAAA3	R620	33/4
SBAA2	R593	33/4
SBAA1	R601	33/4
MAAA10	R602	33/4
MAAA0	R603	33/4
CKEA0	R609	39/4
CKEA3	R572	39/4
CKEA2	R574	39/4
CKEA1	R576	39/4
-CSA3	R578	39/4
-CSA1	R580	39/4
-CSA2	R582	39/4
-CSA0	R584	39/4
MAAA5	R153	33/4
MAAA6	R154	33/4
MAAA9	R155	33/4
MAAA11	R157	33/4
MAAA12	R159	33/4
SBAA0	R161	33/4

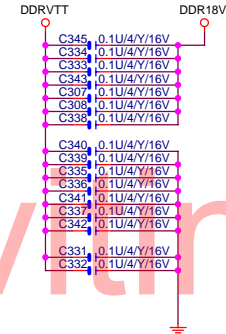
9,14,15	-SCASA	R163	33/4
9,14,15	-SWEA	R165	33/4
9,14,15	-SRASA	R167	33/4

## DDR18V Decouple



SBAA[0:2]	← SBAA[0:2]	9,14,15
-CSA[0:3]	← -CSA[0:3]	9,14,15
CKEA[0:3]	← CKEA[0:3]	9,14,15
MAAA[0..13]	↔ MAAA[0..13]	9,14,15
MODT_A[0..3]	↔ MODT_A[0..3]	9,14,15

## DDRVTT Decouple

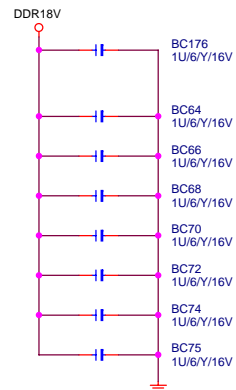


DDRVTT

MAAB1	R616	33/4
MAAB2	R615	33/4
MAAB4	R612	33/4
MAAB3	R597	33/4
MAAB5	R594	33/4
MAAB6	R598	33/4
MAAB13	R617	33/4
MAAB8	R619	33/4
MAAB7	R608	33/4
MAAB9	R600	33/4
MAAB11	R604	33/4
MAAB12	R605	33/4
MODT_B0	R607	39/4
MODT_B1	R608	39/4
MODT_B2	R575	39/4
MODT_B3	R575	39/4
SBAB1	R577	33/4
SBAB0	R579	33/4
MAAB10	R581	33/4
MAAB0	R583	33/4
CKEB0	R585	39/4
CKEB1	R586	39/4
CKEB3	R587	39/4
CKEB2	R588	39/4
-CSB3	R589	39/4
-CSB2	R590	39/4
-CSB1	R591	39/4
-CSB0	R592	39/4
SBAB2	R536	33/4

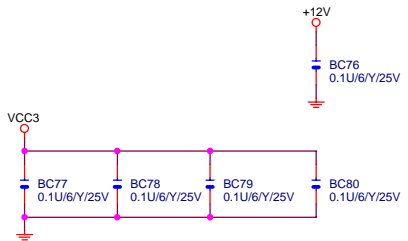
9,16,17	-SWEB	R164	33/4
9,16,17	-SCASB	R166	33/4
9,16,17	-SRASB	R168	33/4

## DDR18V Decouple

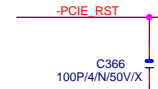
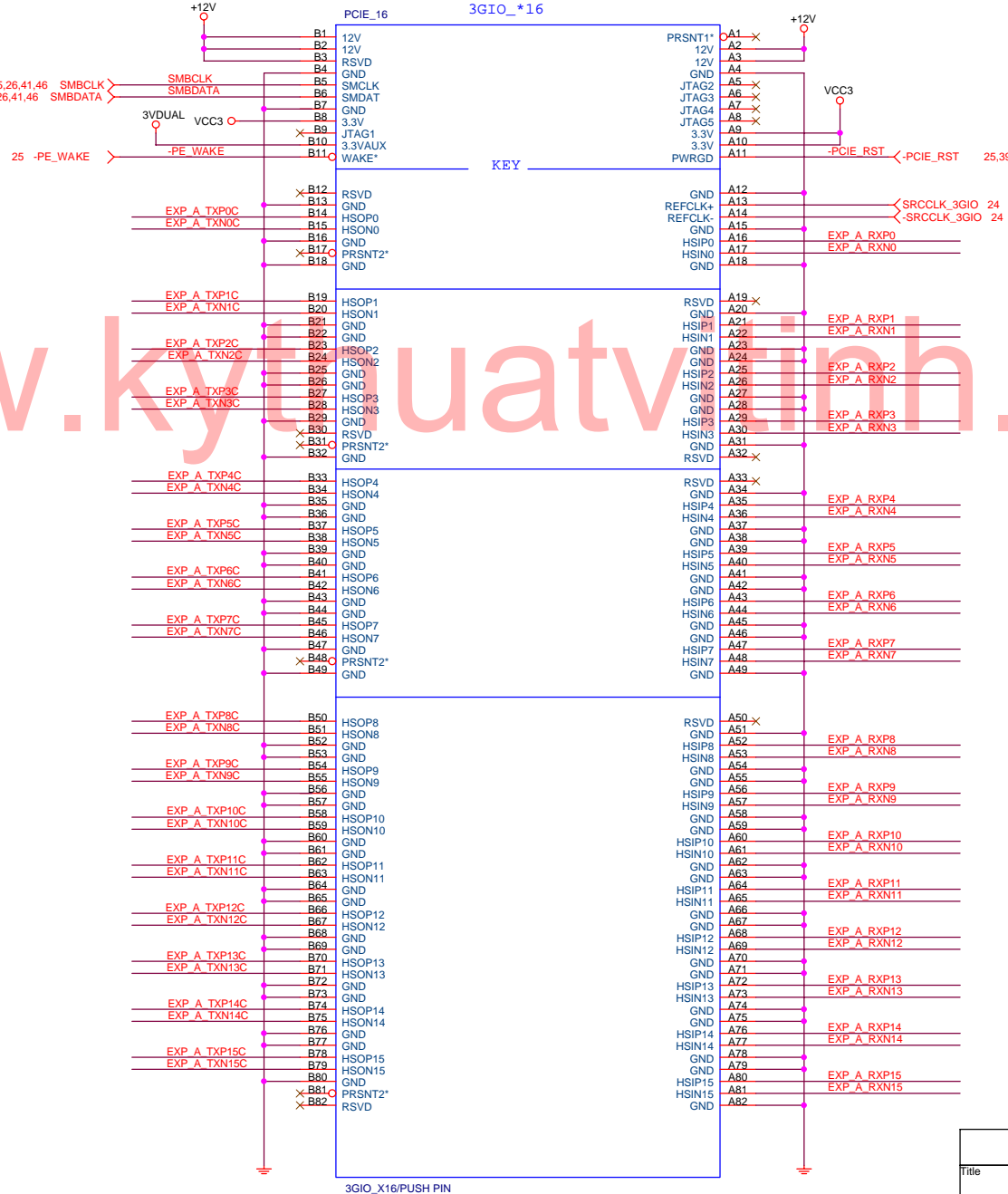


MODT_B[0..3]	↔ MODT_B[0..3]	9,16,17
SBAB[0:2]	← SBAB[0:2]	9,16,17
-CSB[0:3]	← -CSB[0:3]	9,16,17
CKEB[0:3]	← CKEB[0:3]	9,16,17
MAAB[0..13]	↔ MAAB[0..13]	9,16,17

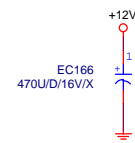
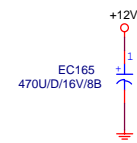
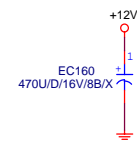
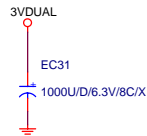




14,15,16,17,21,24,25,26,41,46 SMBCLK  
14,15,16,17,21,24,25,26,41,46 SMBDATA

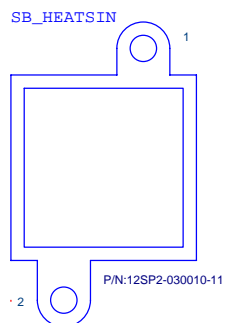
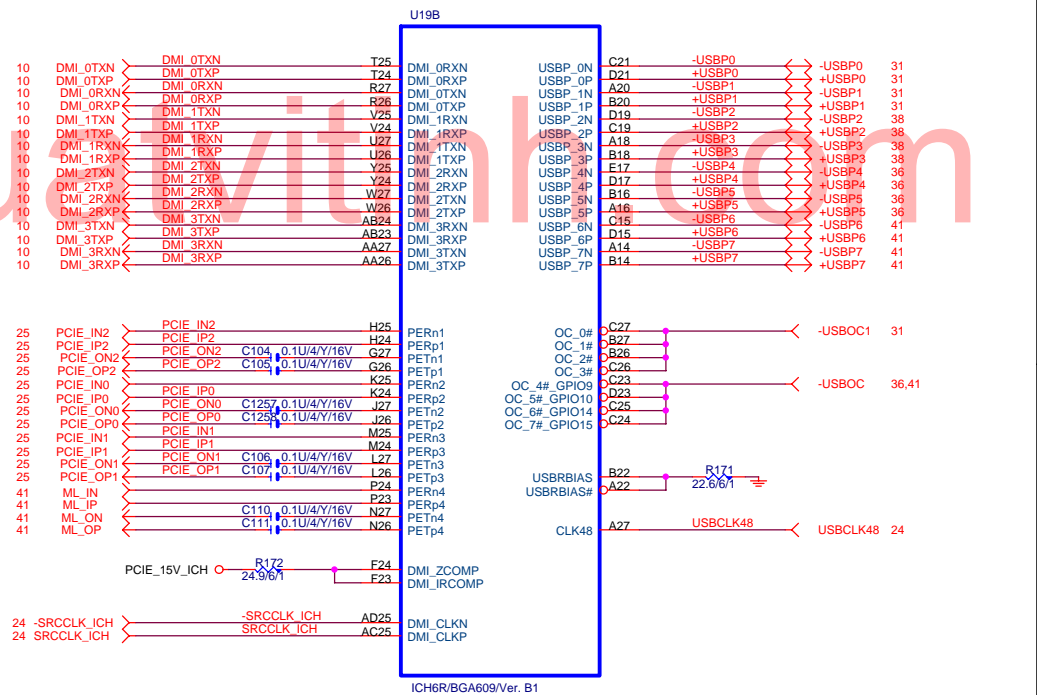
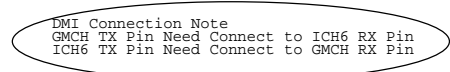


EXP A RXP[0..15] >>> EXP\_A\_RXP[0..15] 10  
EXP A RXN[0..15] >>> EXP\_A\_RXN[0..15] 10



3GIO\_X16/PUSH PIN





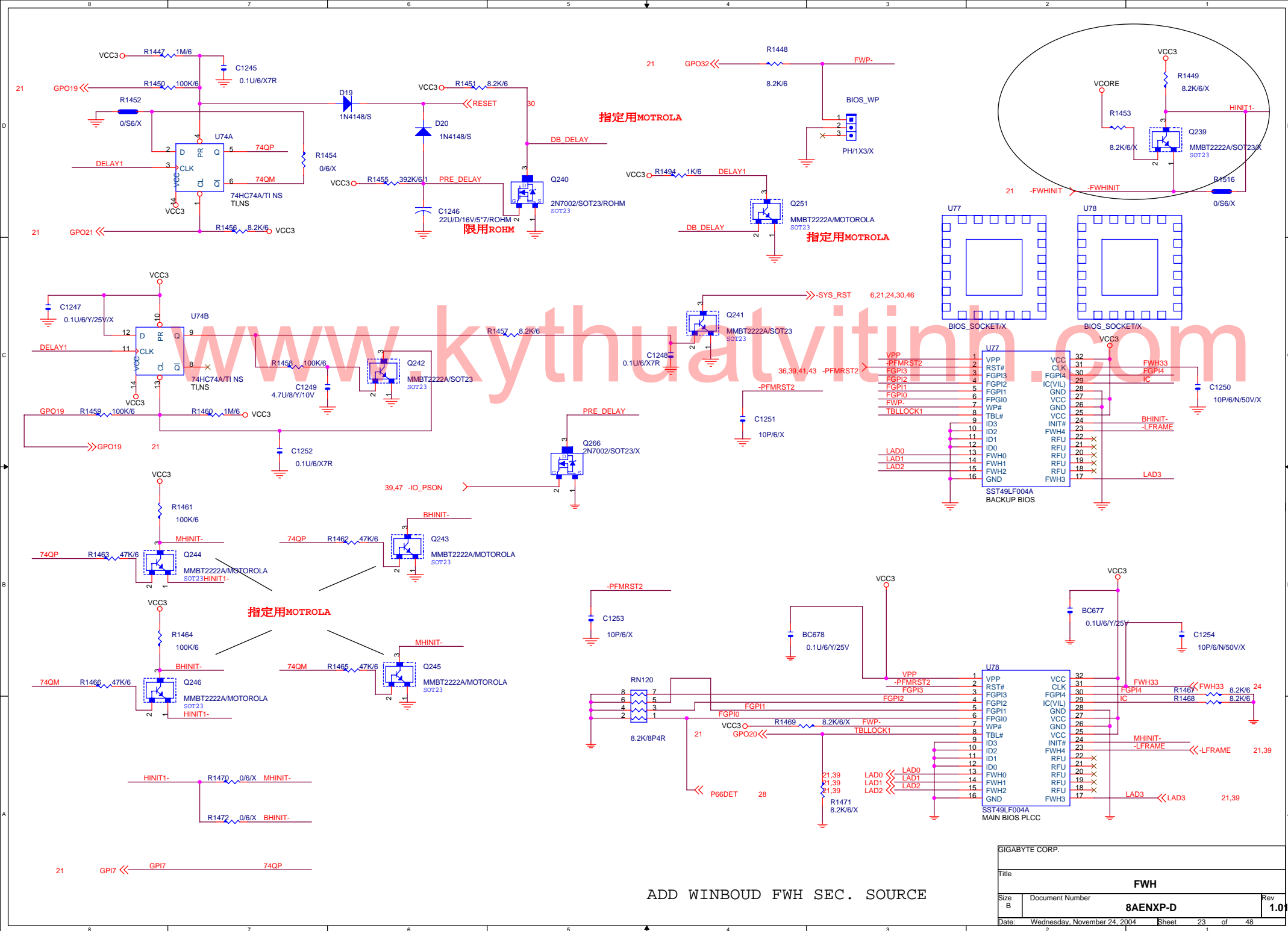








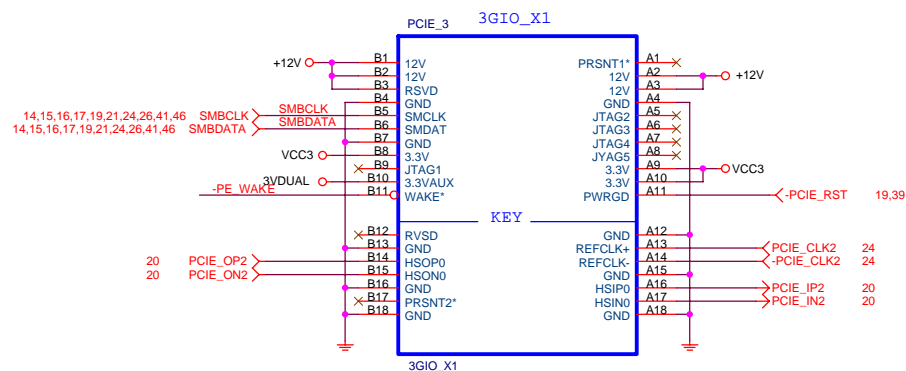






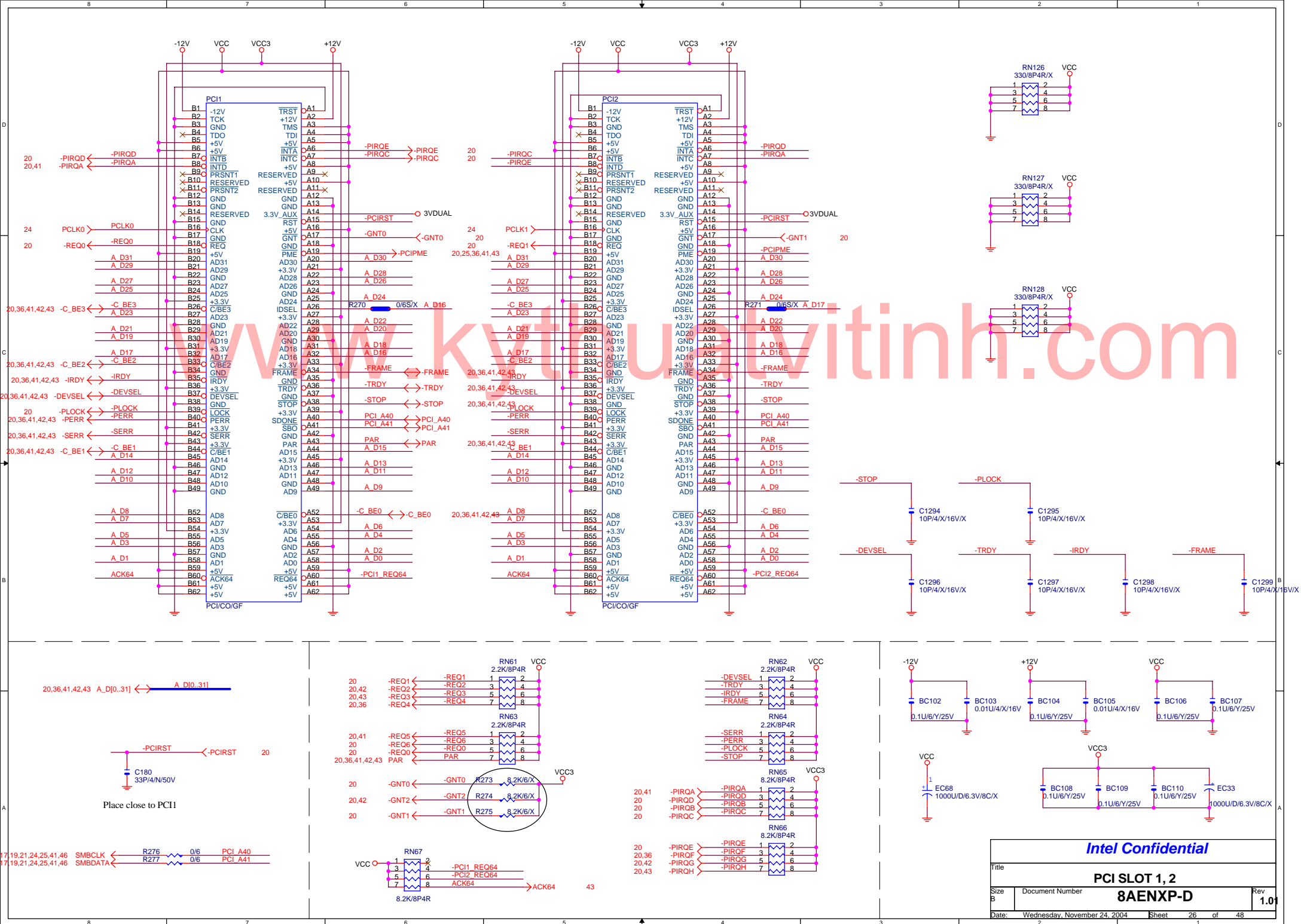




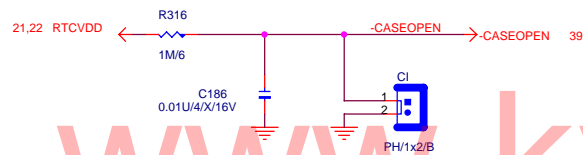
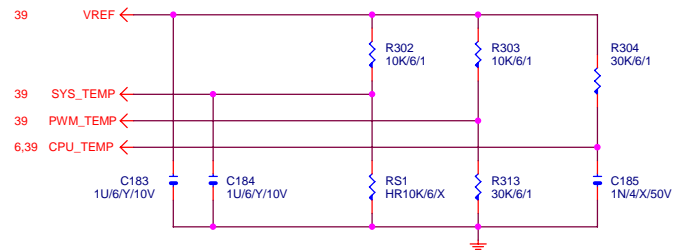


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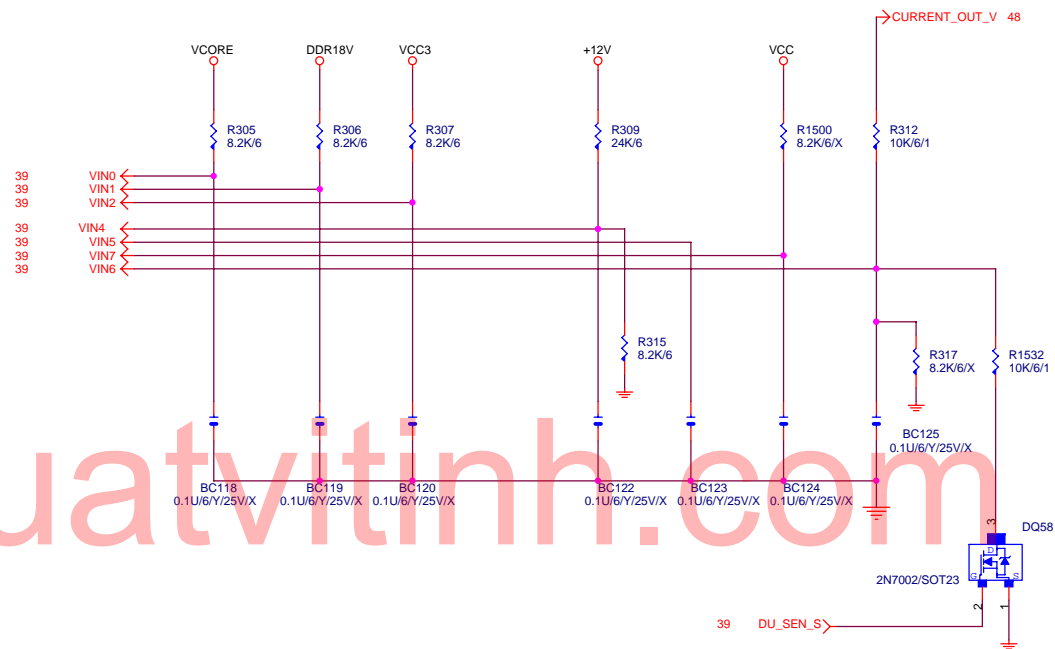




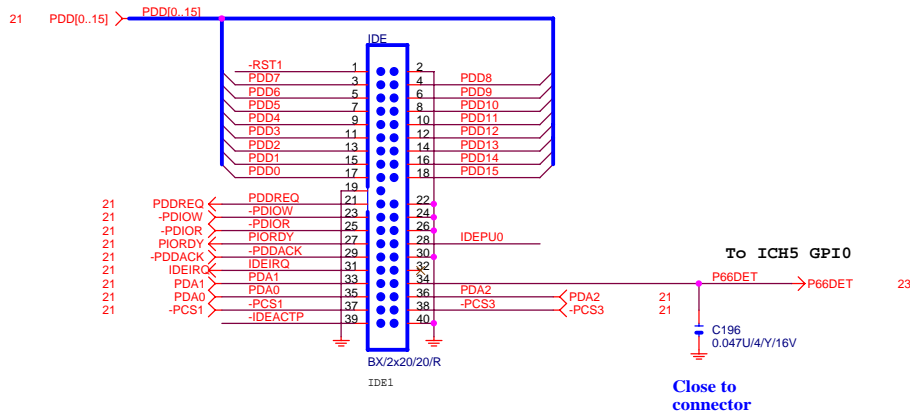
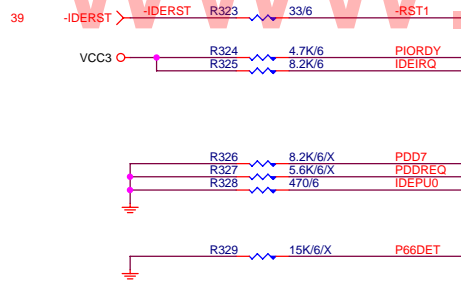
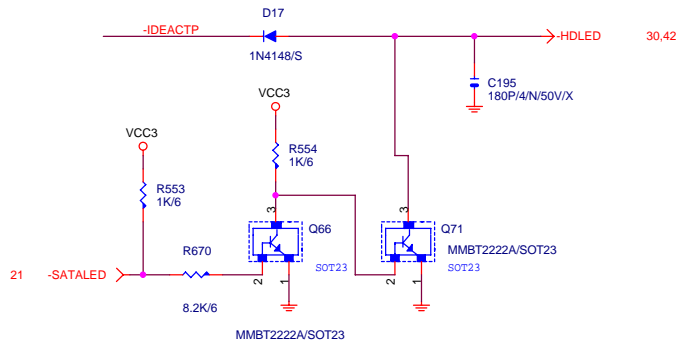




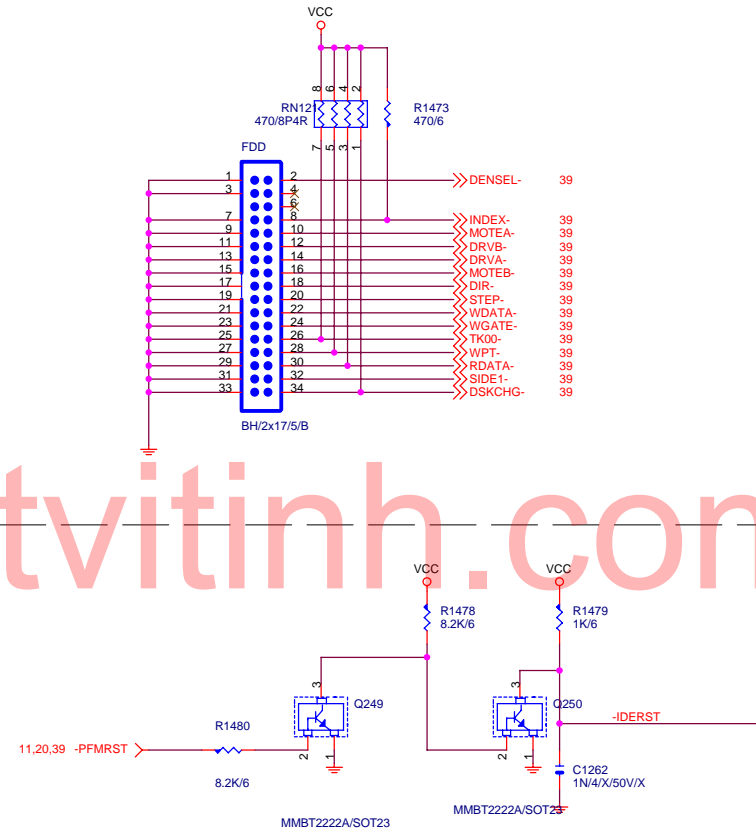
Case Open Circuits



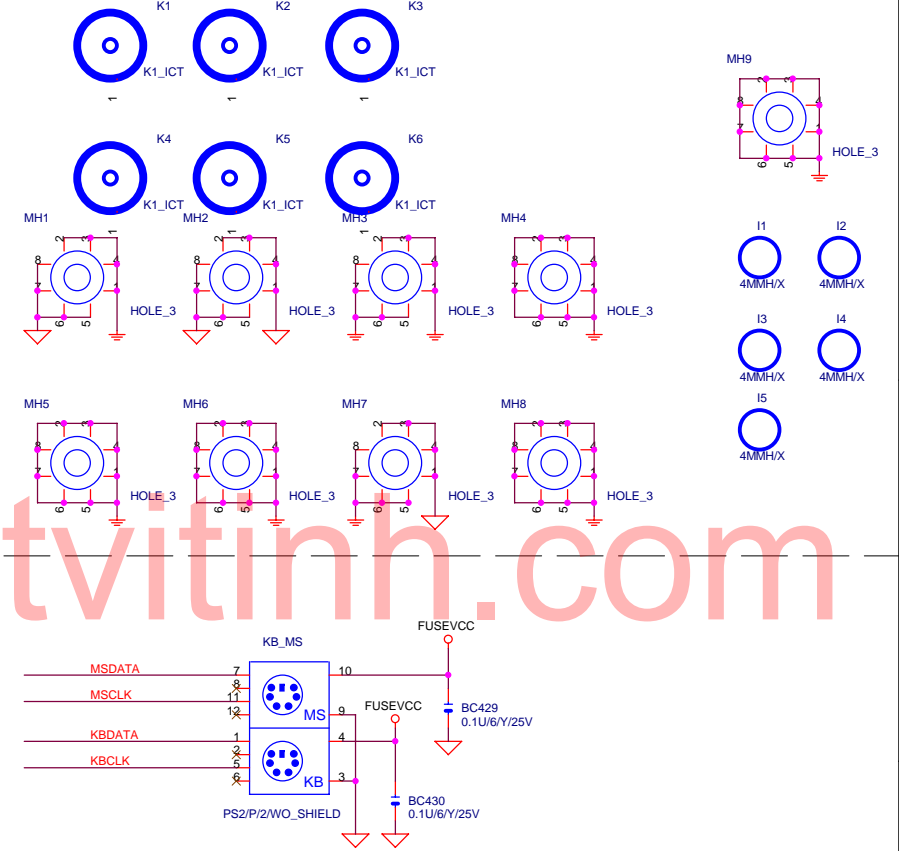
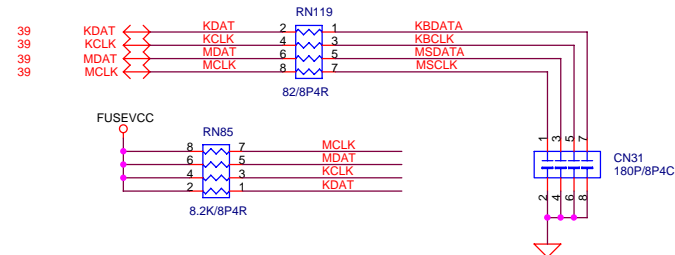
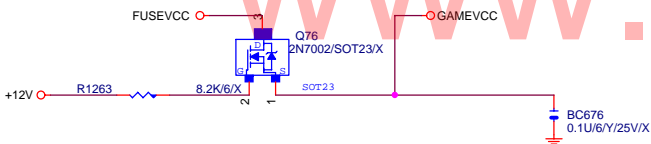
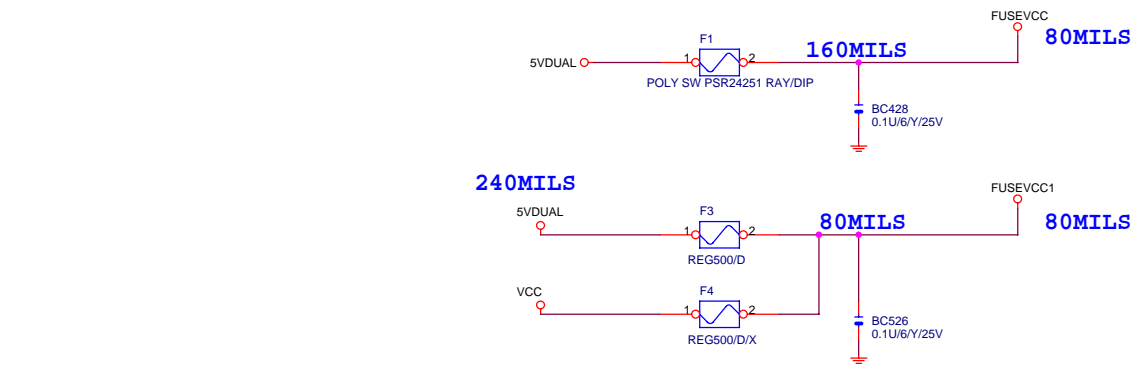




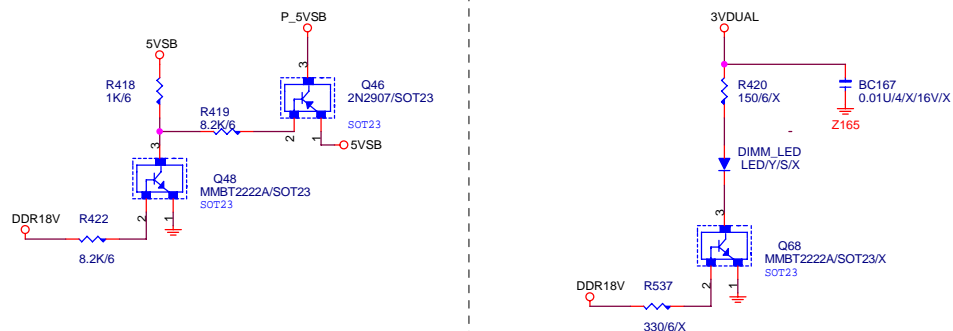
PRIMARY IDE CONNECTOR







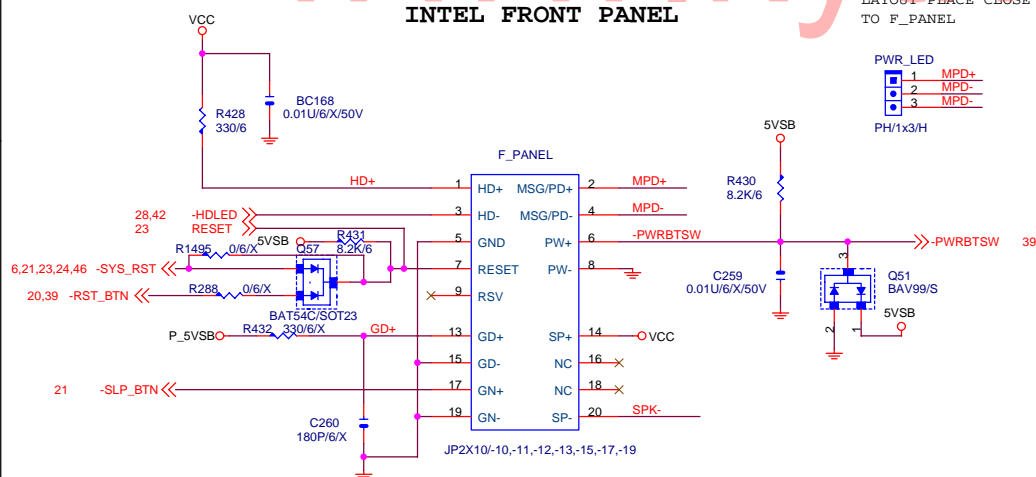




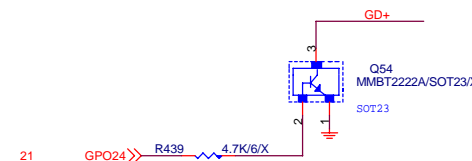
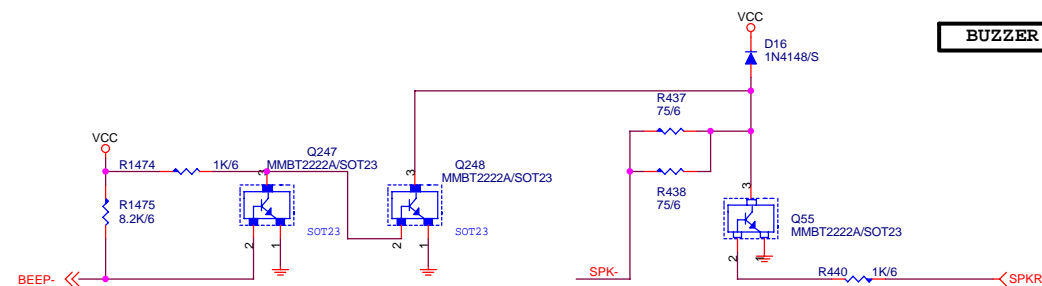
## INTEL FRONT PANEL

3 PIN POWER LED  
LAYOUT PLACE CLOSE  
TO F\_PANEL

PWR\_LED  
1 MPD+  
2 MPD-  
3 MPD-  
PH/1x3/H



## BUZZER



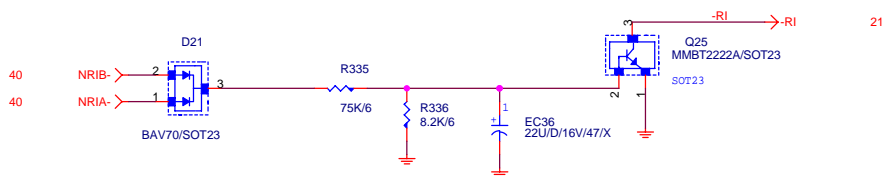
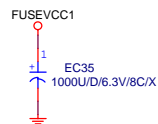
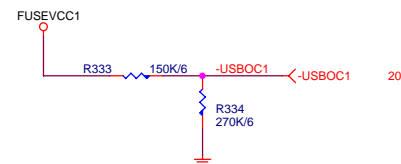
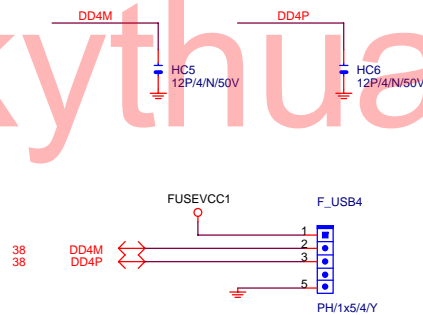
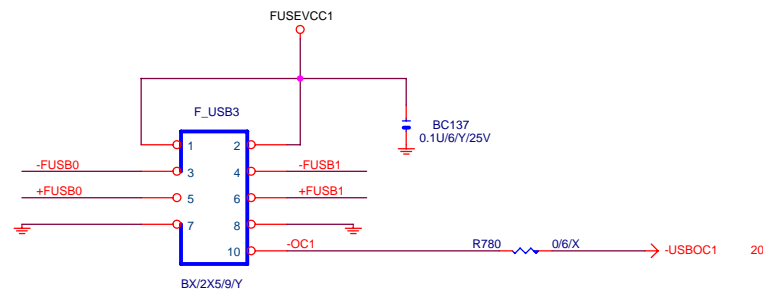
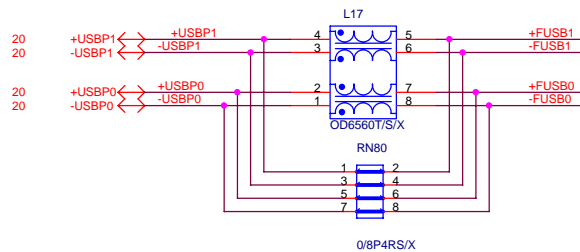
Intel Confidential

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FRONT PANEL			
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Custom			
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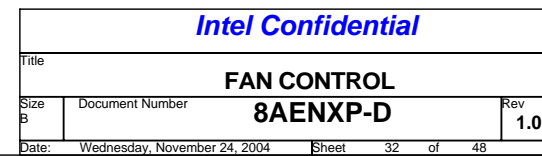
# FRONT USB

## ICH5 USB2.0



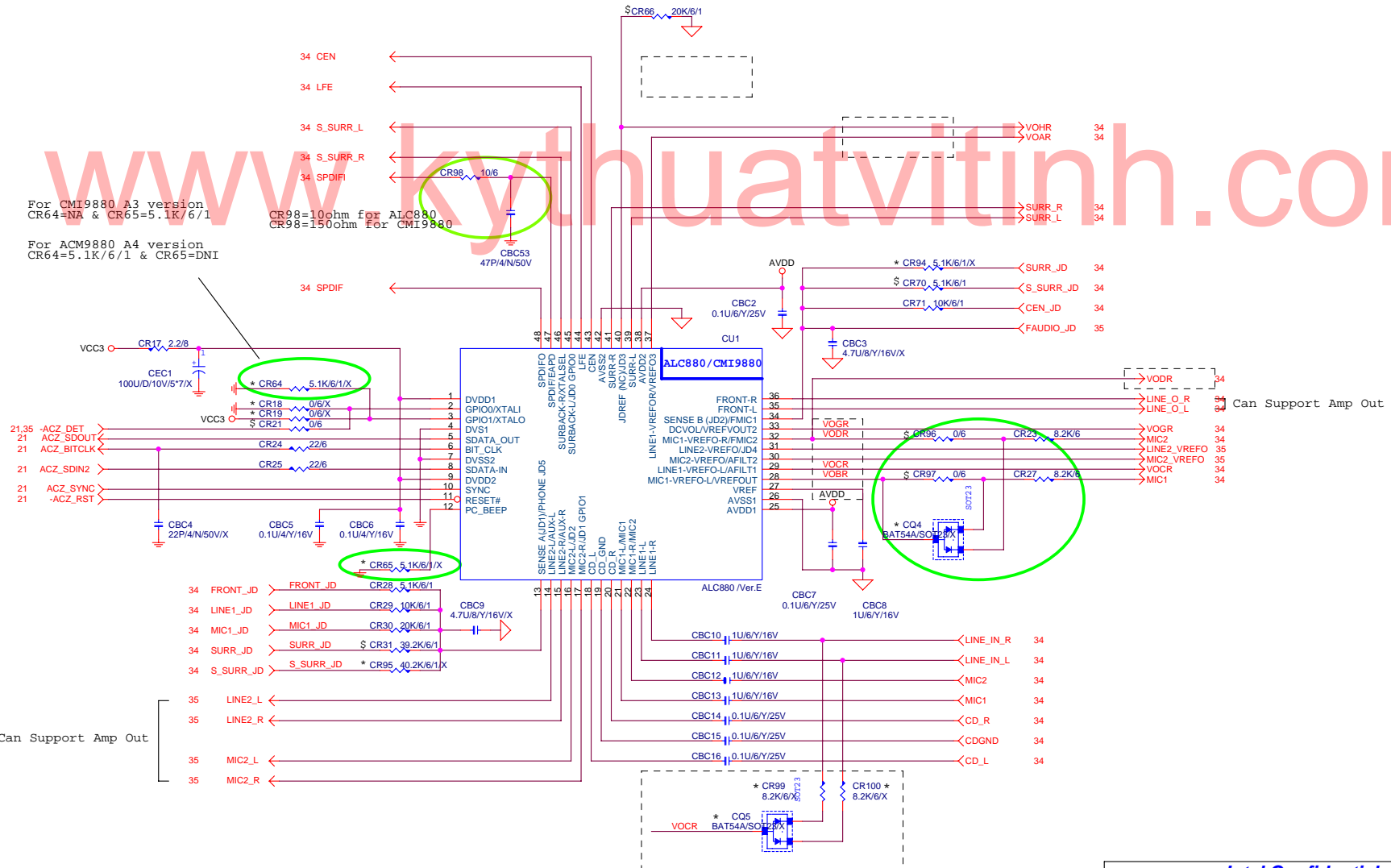
Intel Confidential			
Title			
FRONT USB CONNECTOR			
Size			
Document Number			
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1.01			
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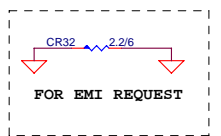
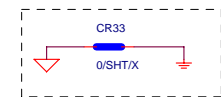




"\$" means for ALC880 only  
 "\*" means for CMI9880 only

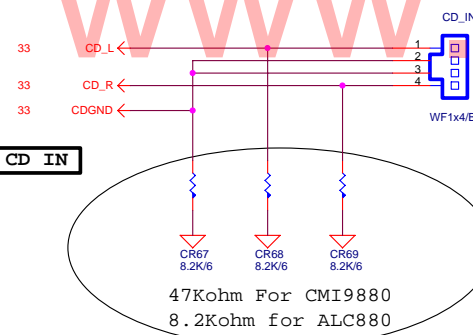
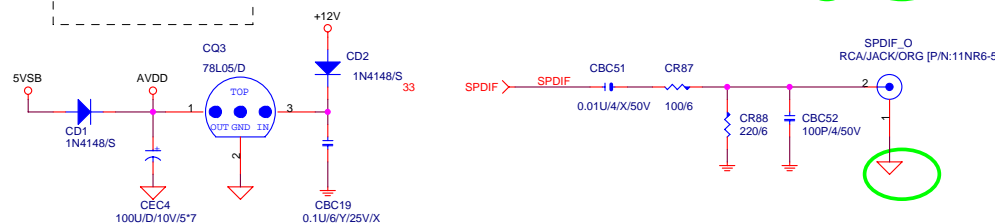






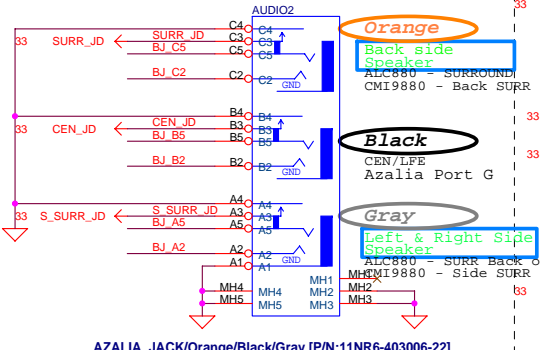
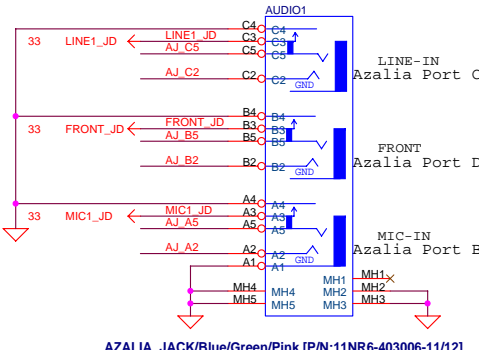
When CMI9880  
CR84 = 150ohm  
CR86 = 150ohm  
CR93 = 47K ohm

When ALC880  
CR84 = 8.2Kohm  
CR86 = 8.2Kohm  
CR93 = DNI



Azalia Jack  
Normal --- pin4/pin3 open  
Plug jack --- pin4/pin3 close

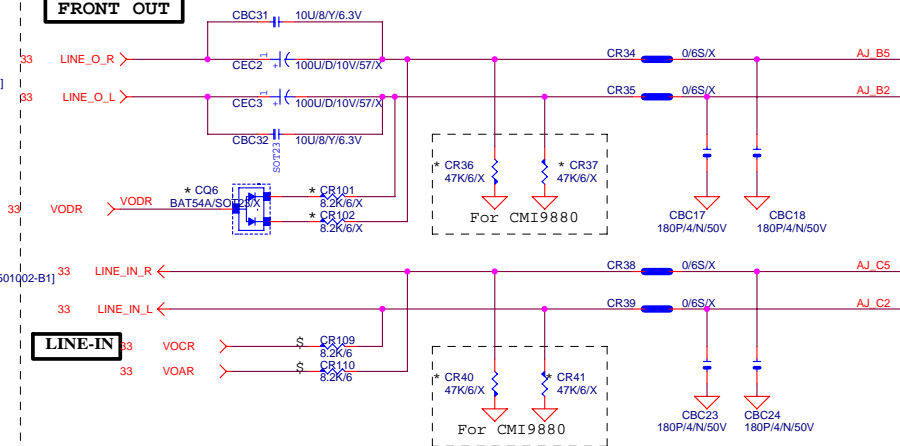
CMI9880 Port A is Side SURROUND, Port H is Back SURROUND  
ALC880 Port A is SURROUND, Port H is SIDE



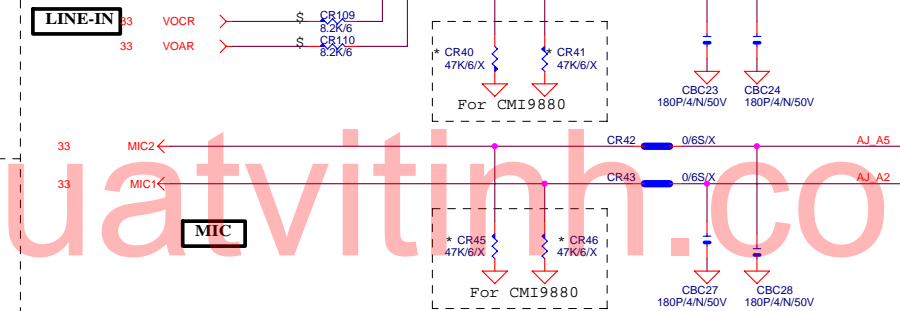
AZALIA\_JACK/Blue/Green/Pink [P/N:11NR6-403006-11/12]

AZALIA\_JACK/Orange/Black/Gray [P/N:11NR6-403006-22]

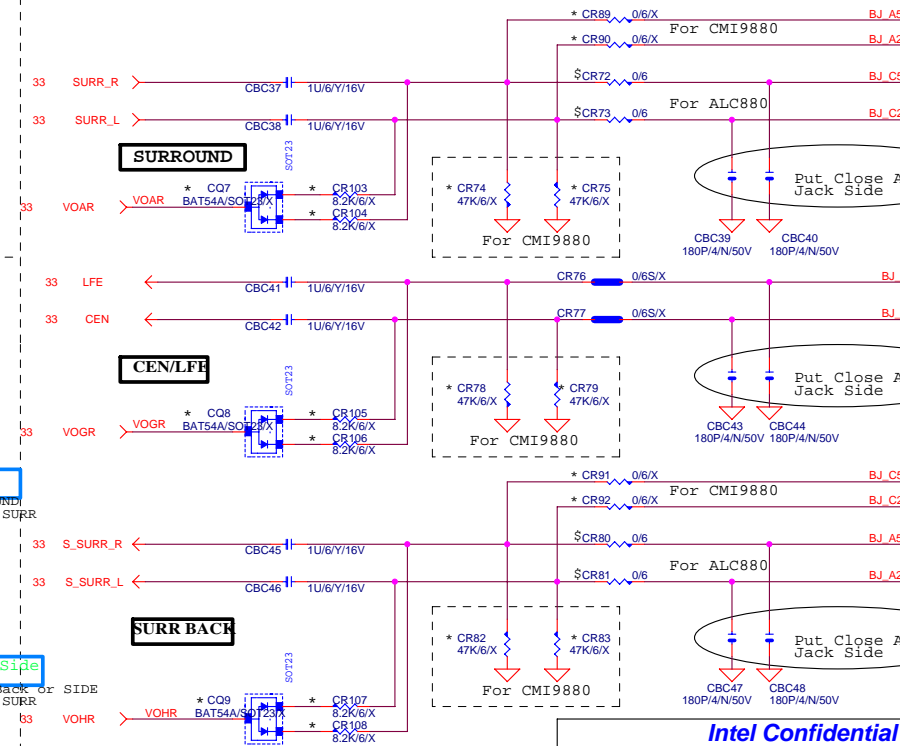
# LINE OUT FRONT OUT



## LINE-IN



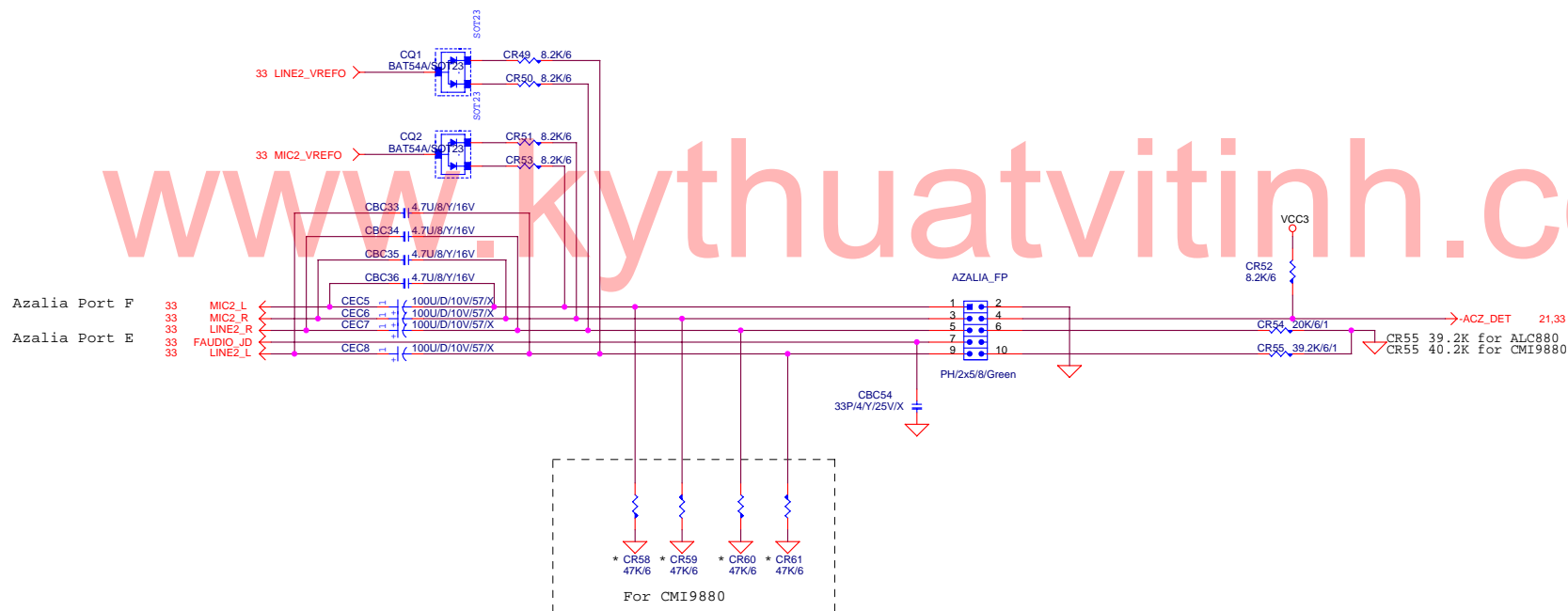
## MIC



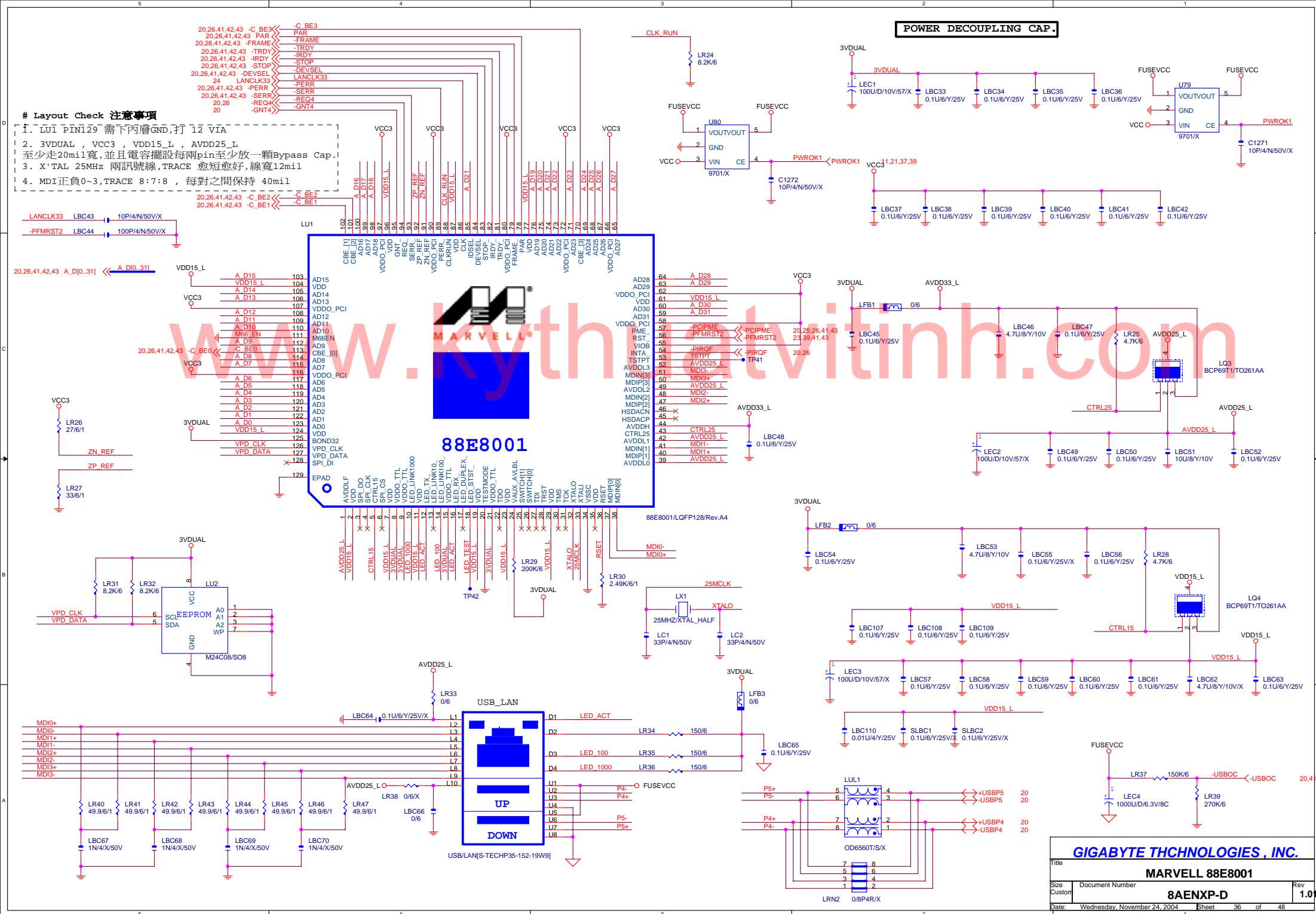
Intel Confidential

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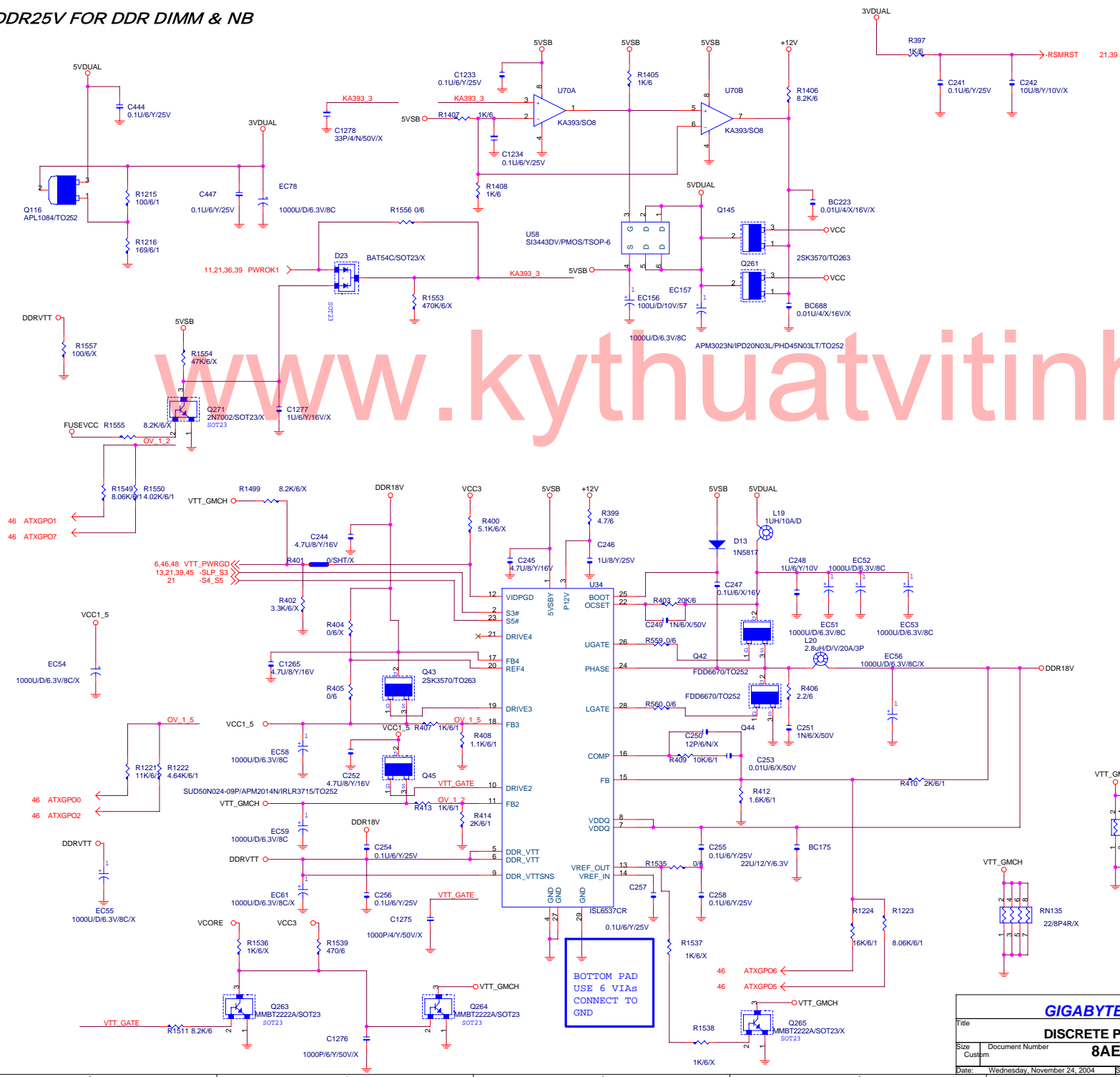








*DDR25V FOR DDR DIMM & NB*



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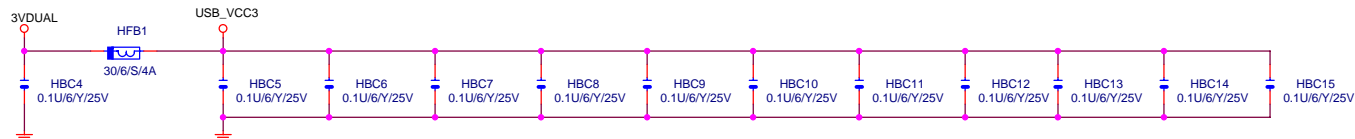
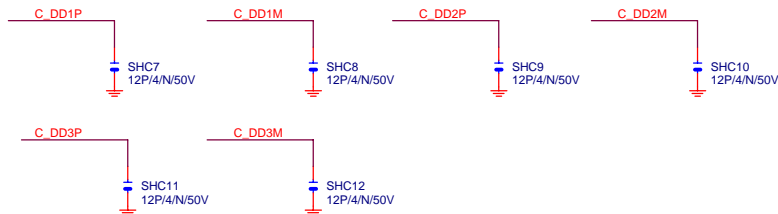
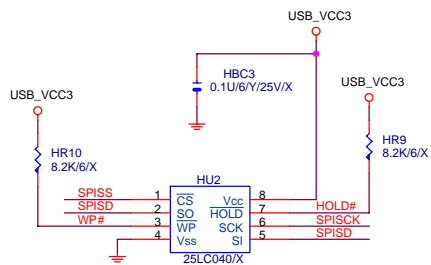
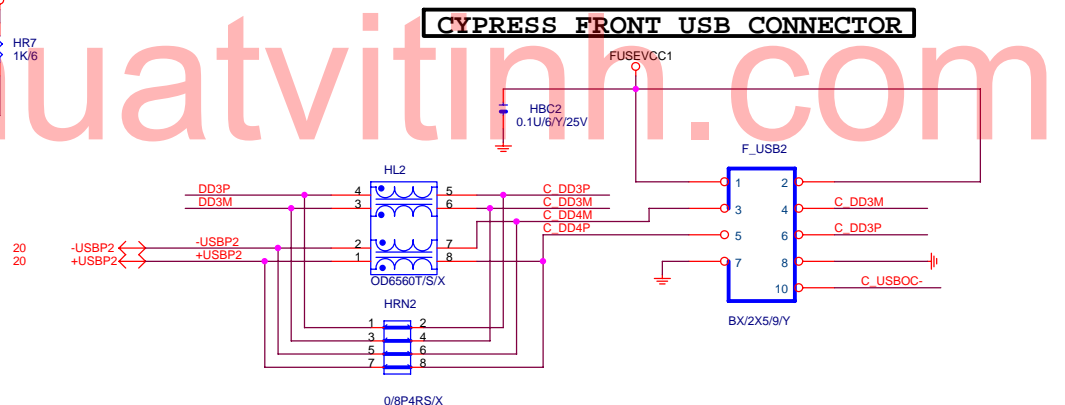
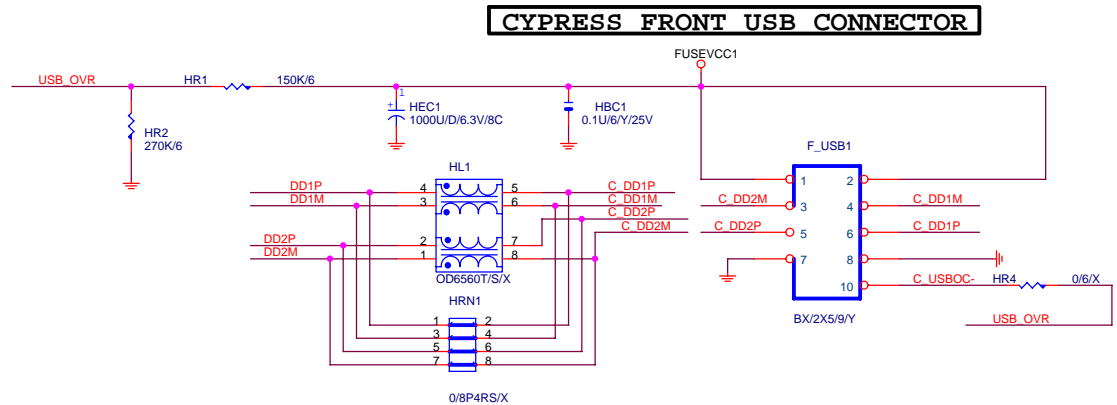
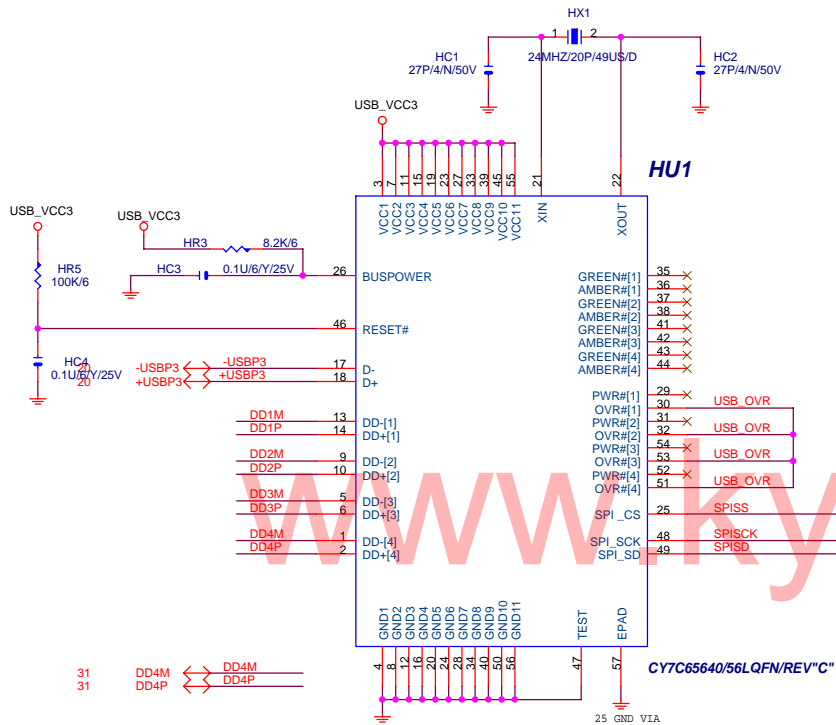
## DISCRETE POWER

**8AENXP-D**

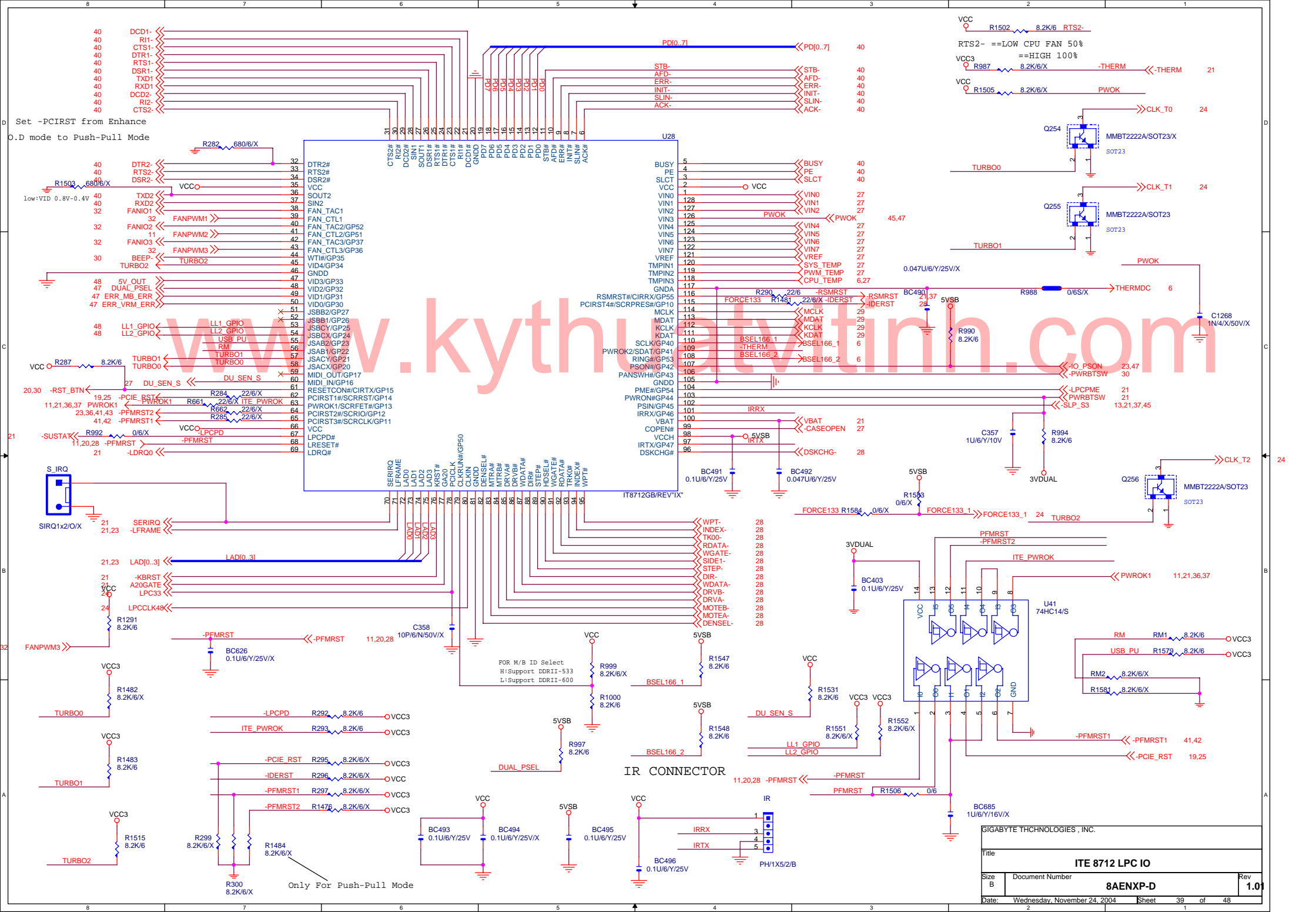
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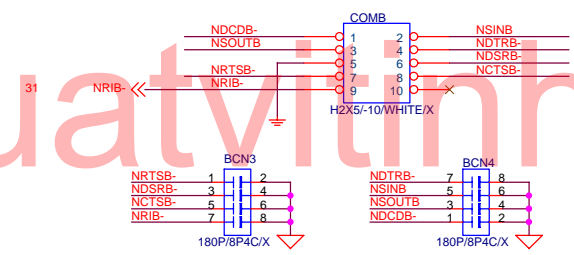
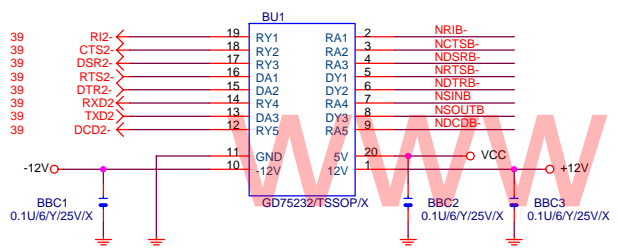
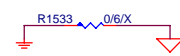
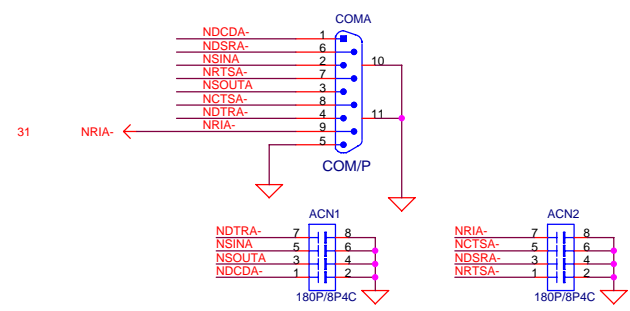
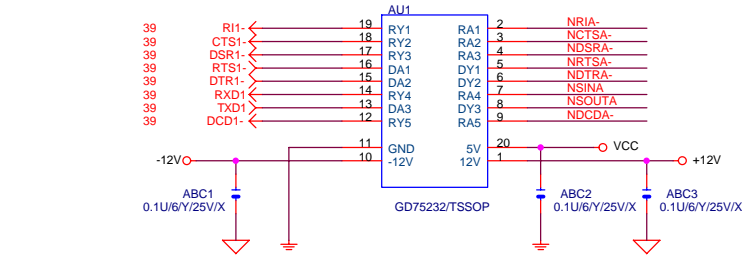




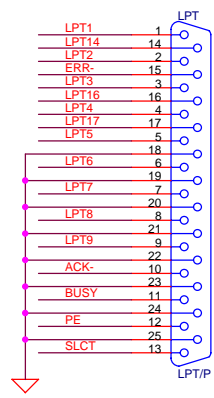
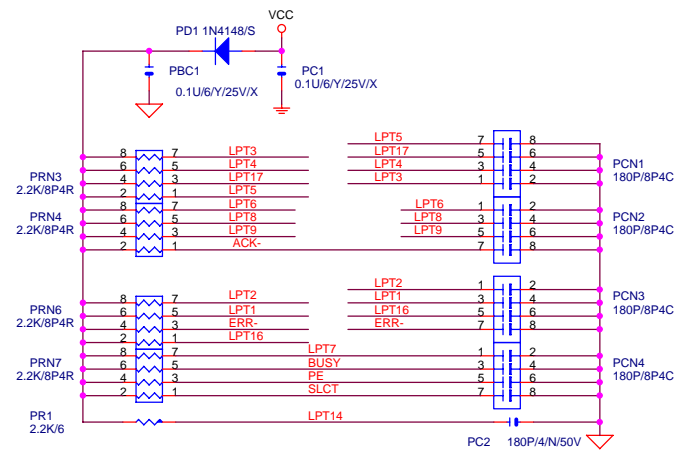
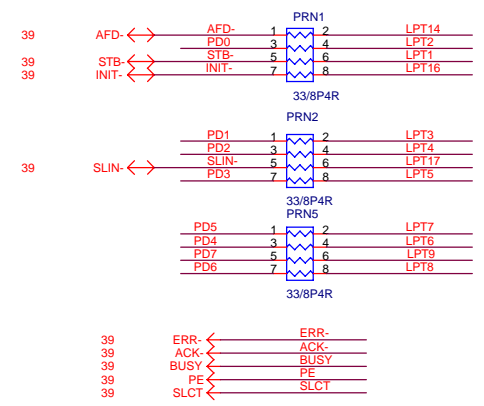




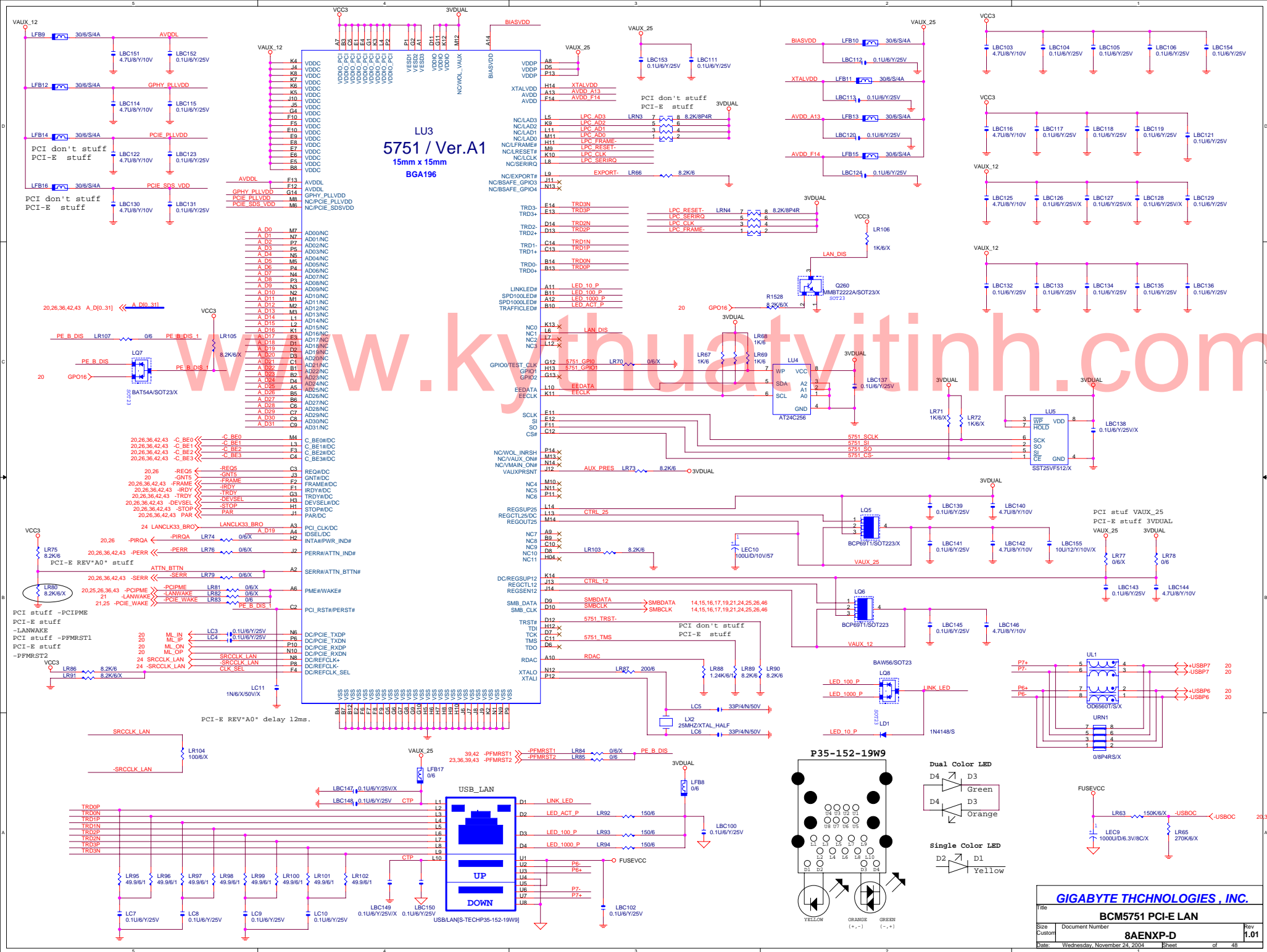




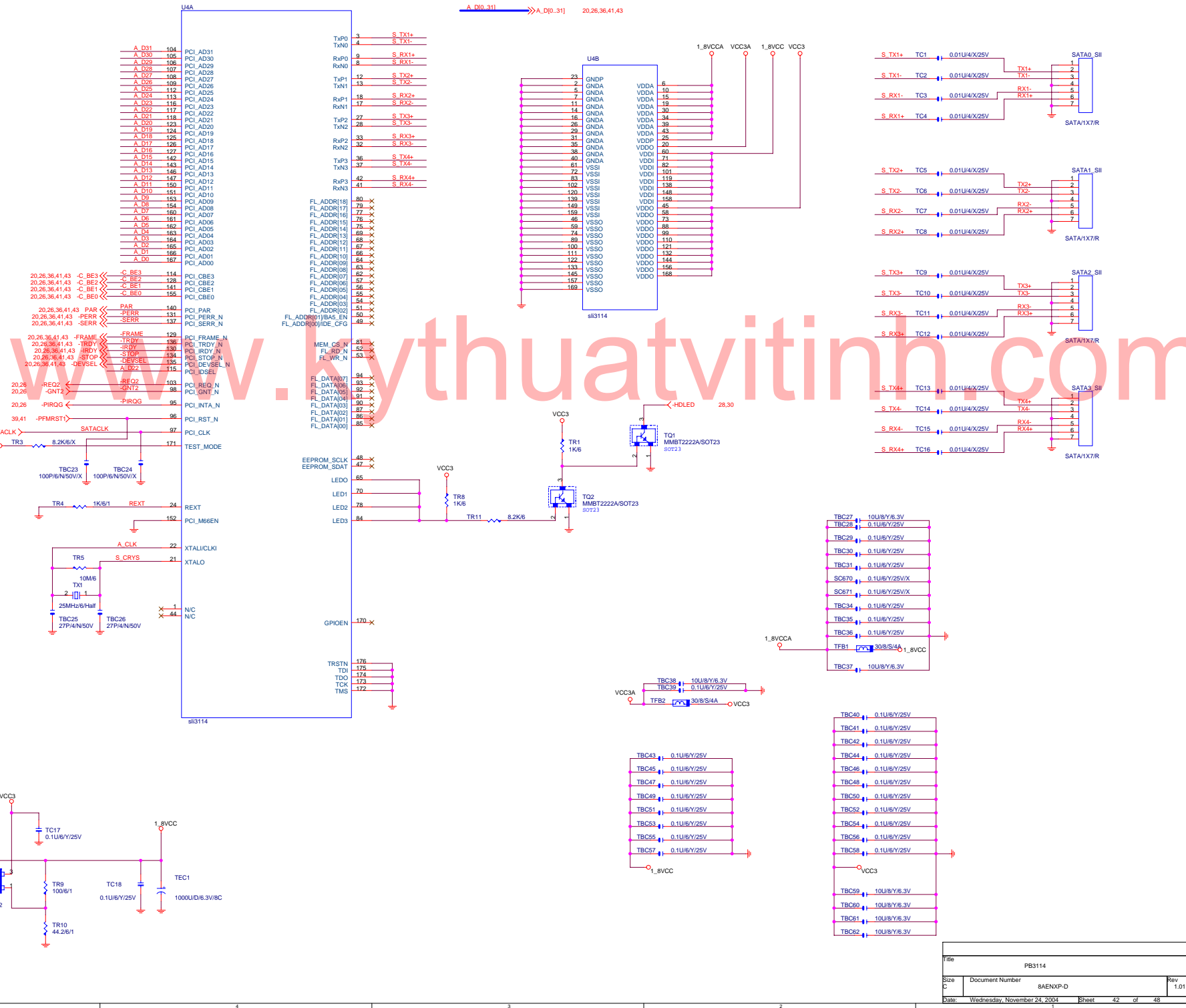
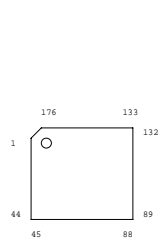
39 PD[0..7] <-> PD[0..7]





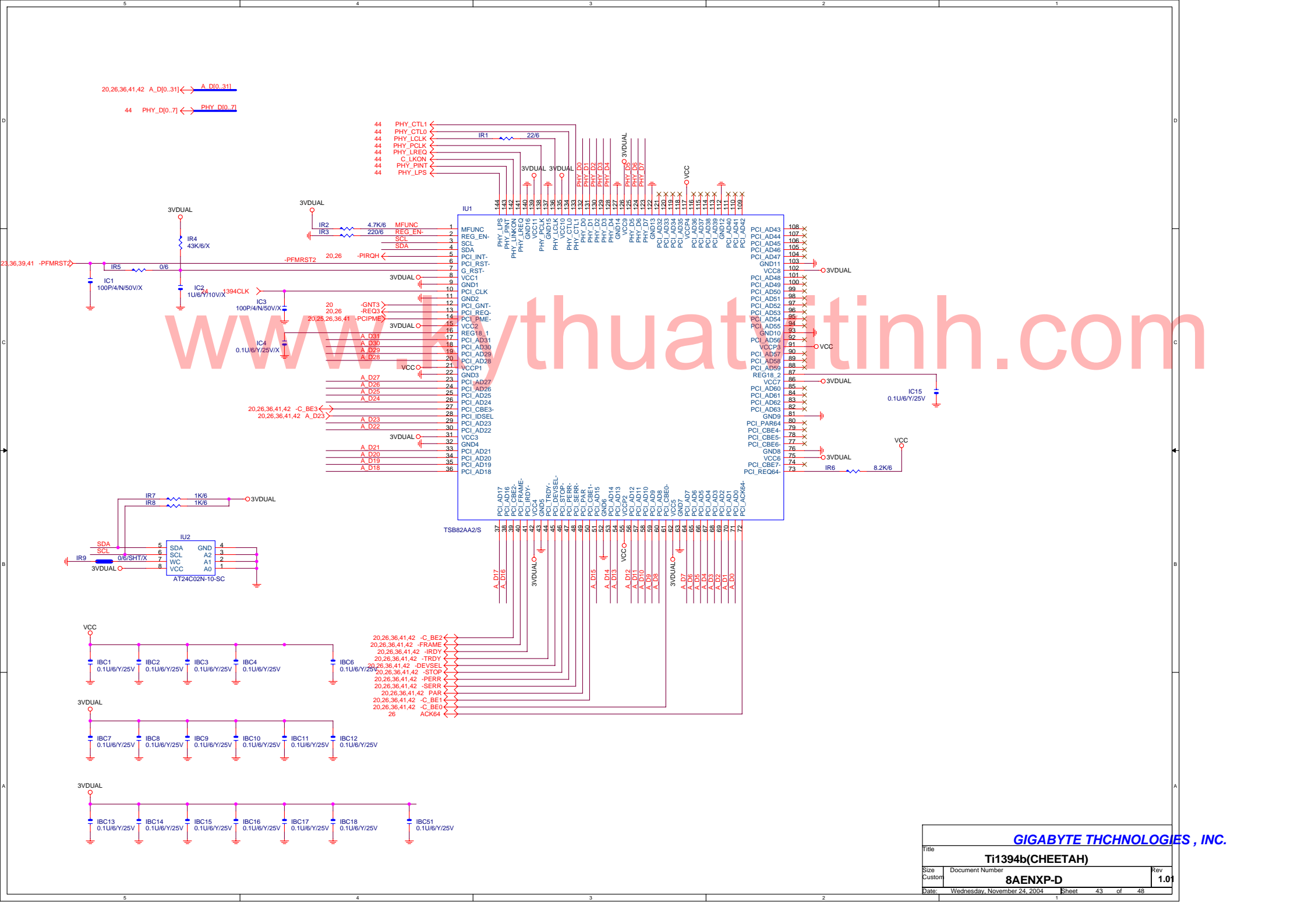




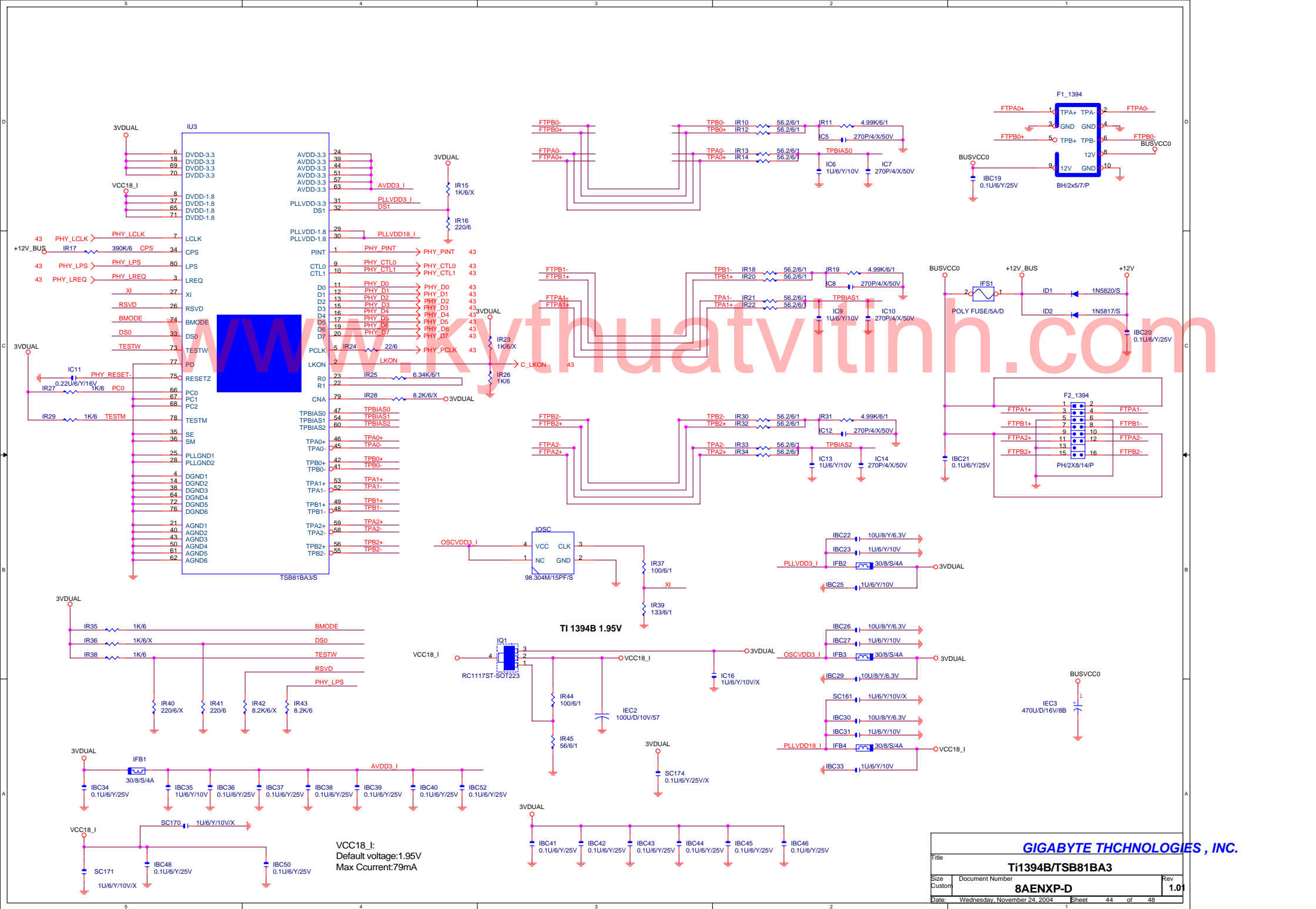


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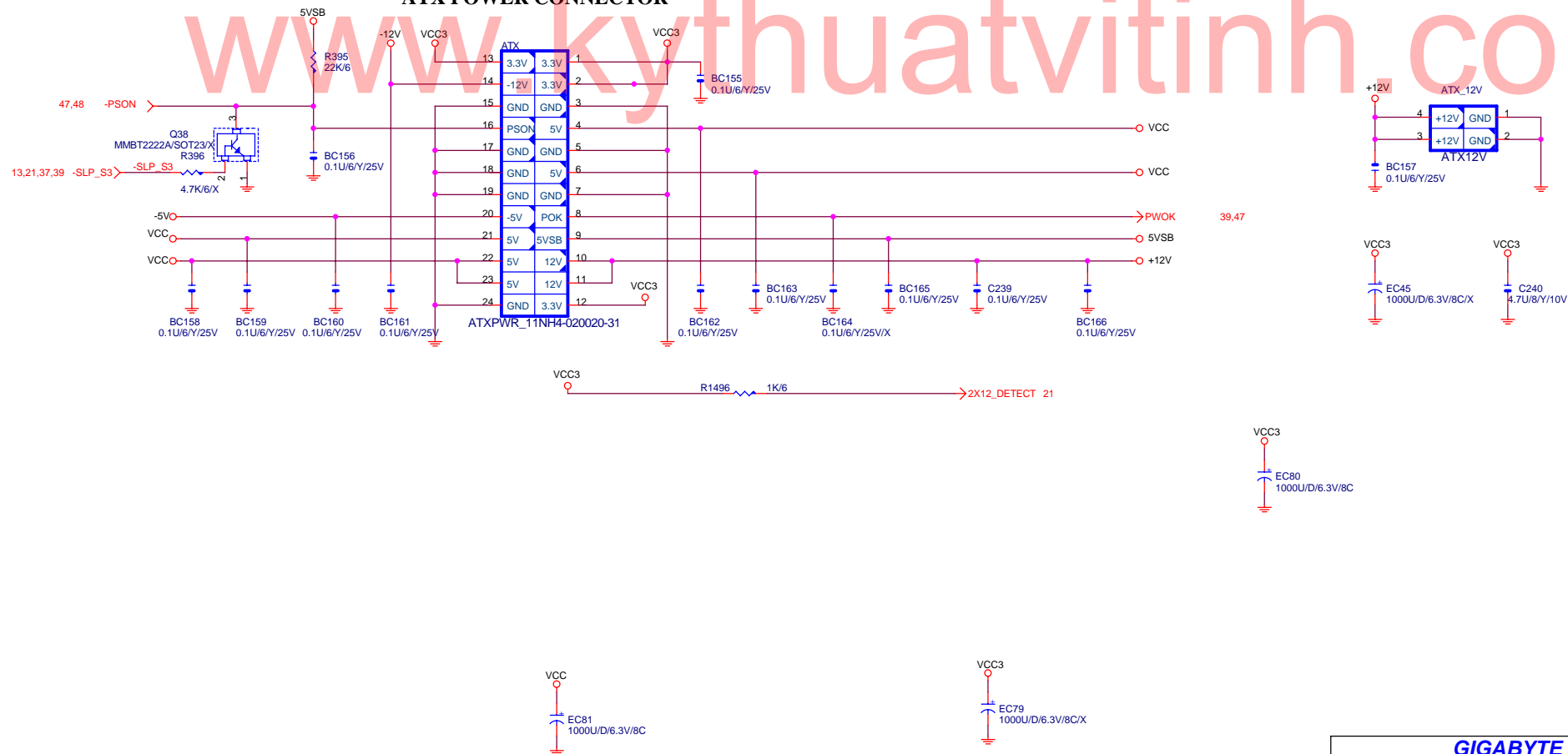








# ATX POWER CONNECTOR



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